Assessment of Inverter-based Distributed Generation Induced Ground Fault Overvoltage on Delta-Wye Substation Transformers

Interconnection Technical Working Group

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Albany, New York

About Pterra

- Consulting firm specializing in analytical studies and assessments of transmission and distribution systems
- Established in 2004
- Based in Albany, NY
- Has conducted over 300 studies of distributed generation in various states

Overview

- Pterra was contracted by NYSERDA to provide consulting services to the NYS Department of Public Service in relation to the SIR application inventory SIR - Standardized Interconnect Requirements
- One of the issues that Pterra was asked to address was the need for 3V0 mitigation for potential overvoltage impacts from inverter-based DG

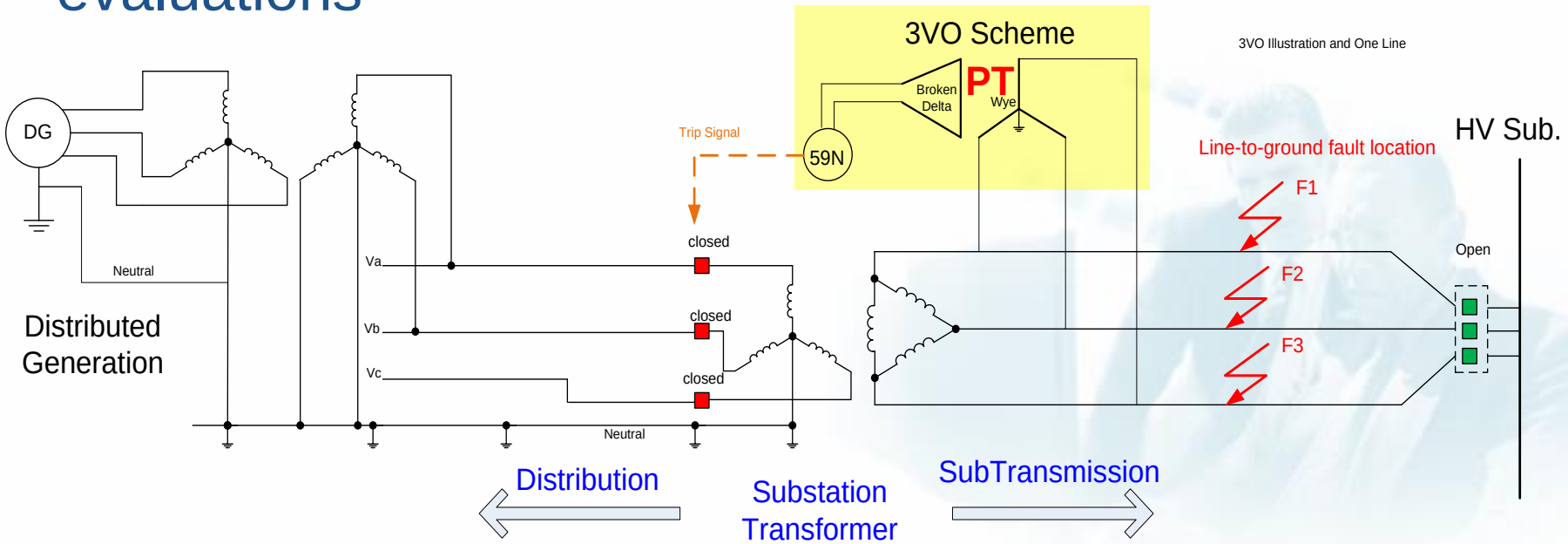
Scope

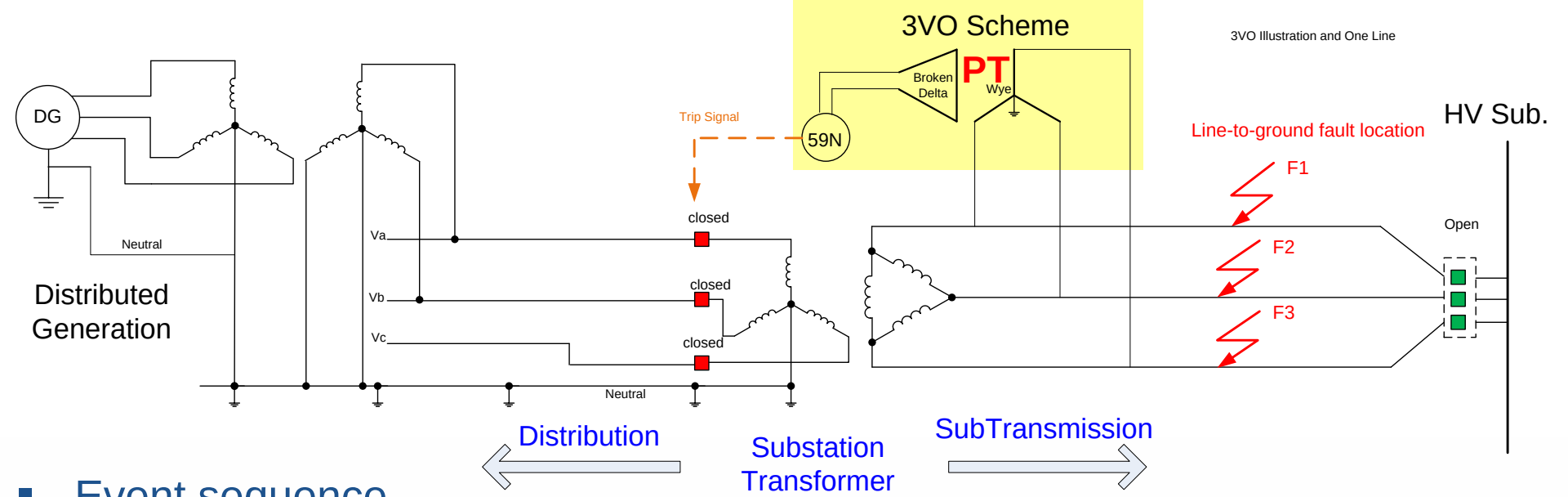
- Pterra proposed a multi-phase research effort of which this report is Phase I
- Phase I Scope:
  - Confirm the potential for Ground Fault Overvoltage (GFOV)
  - Identify the conditions when such a potential may be present
- Phase II Scope (not yet conducted):
  - Identify and test potential mitigation measures

Background-GFOV and 3VO

- Potential GFOV may be found in specific configurations. This study evaluated a typical configuration identified in SIR evaluations

- Configuration:
  - Subtransmission line
  - Serving Delta-wye-grounded substation transformer
  - DG installed on the distribution feeder





- Event sequence
  - SLG fault occurs on subtransmission
  - Fault detected
  - Subtransmission breaker opens islanding the faulted line and distribution feeders with DG
  - DGs on the island do not trip fast enough
  - Not enough load on the island to depress voltage
  - Overvoltage occurs on the subtransmission line

- Need for 3V0
  - One mitigation measure is to add PTs on the transformer delta (high) side
  - The PTs measure the 3V0 voltage to identify an overvoltage
  - Relays send signals to trip DG or other breakers to eliminate the overvoltage

Normally, the three winding voltages of a transformer add vectorially to zero. When ground faults occur, the voltage that appears corresponds to 3 times the zero-phase-sequence component of any one of the three phase-to-ground voltages at the potential-device location. This voltage is referred to as "3V0 " and is the basis for certain types of protective relaying schemes.

Phase I Findings

- GFOV is possible in the studied configuration
  - 2 of 3 inverter-based DG models were found able to excite the high side of transformer to high voltage
- Magnitude of overvoltage depends on
  - Ratio of DG to load on the island
  - Performance of surge arresters when present
  - Interaction of different manufacturer designs for inverter controls in the island
- When calculating load on the island, include all load downstream from the opened breaker
  - Include subtransmission loads

Phase I Findings

- Penetration levels in terms of DG/load ratios where GFOV potential is insignificant (based on conservative assumptions and an idealized configuration)
  - 65% - if criteria is to limit voltage to 1.38 pu
  - 100% - if criteria is to avoid arrester failure, assuming arresters are the first protection against overvoltage
- If the above levels are exceeded, additional assessment is needed on a case-by-case basis to test the actual island configuration/s and performance of active islanding, among others. This study presents an approach to conducting the additional assessment.

According to ANSI/IEEE C62.92, the GFOV for an effectively grounded system is to be limited to 138%. This is assumed to be the same limiting value for ungrounded systems.

Next Phase of the study is to identify and test feasible mitigation measures should a GFOV potential be determined.

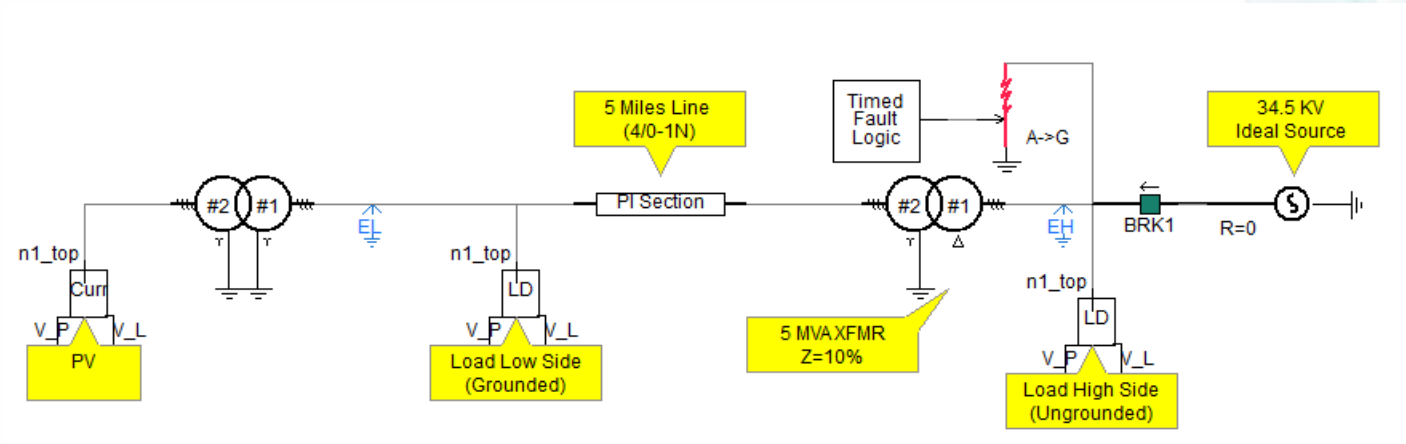
Assumptions

- To obtain conservative results, active anti-islanding protections in inverters and non-linearity of transformers (magnetizing and saturation) were deactivated in all scenarios
- Grid was modeled with the ideal source
- For conservatism, a reactive portion of the load is tuned to minimize reactive power mismatch in the island
- Load's active power was varied based on the desired penetration level in each scenario
- Current chopping limit of circuit breaker is zero amps

Methodology

- Time domain simulation software (PSCAD™) is used for the assessment

- Three inverters used for the study are commercially available
  - Inverter#1: 250 kW, three-phase, UL-1741 certified
  - Inverter#2: 250 KW, three-phase, UL-1741 certified
  - Inverter#3: 1 MW, three-phase, UL-1741 certified



Methodology

- Total of 28 scenarios or 74 cases performed in this study

- Categorized to three groups for clarity

  - **Group 1 / Table 1 (Scenario 1 through 15).** The objective of these scenarios is to illustrate critical penetration level for different inverters, load locations, and DG to load ratio.

  - **Group 2 / Table 3-2 (Scenario 16 through 23).** The objective of these scenarios is to study the impact of the surge arresters in relation to the GFOV as well as to demonstrate the capability of the surge arresters in handling the GFOV.

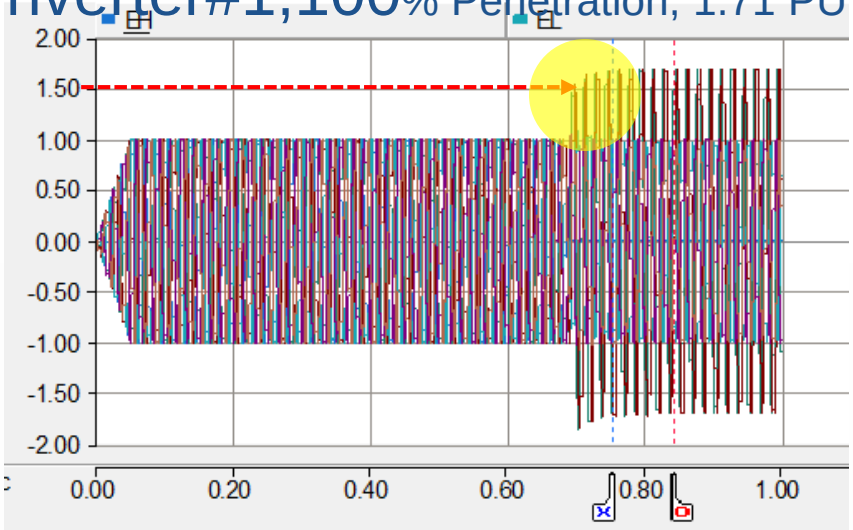
  - **Group 3 / Table 3 (Scenario 24 through 28)** are intended to study the impact of modeling the high-quality load factor.

Simulation Results

- **Group 1 / Table 1 (Scenario 1 through 15).** The objective of the scenarios in this group is to illustrate critical penetration level for different inverters, load locations, and penetration level.

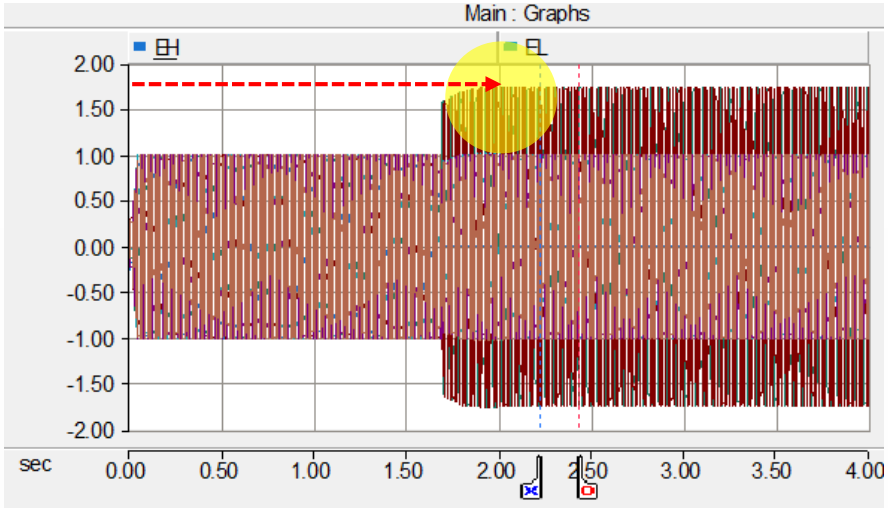
Scenario	DG/LD_L[1] %	DG/LD_H[2] %	DG/(LD_L+LD_H) %	Over Voltage (Steady State)		
				Inverter#1	Inverter#2	(Inverter#3)
1	50			1.2	N/A[3]	N/A
2	65			1.38	N/A	N/A
3	90			1.62	N/A	N/A
4	100			1.71	N/A	1.73
5	105			1.75	N/A	1.78
6		50		1.2	N/A	N/A
7		65		1.38	N/A	N/A
8		90		1.62	N/A	N/A
9		100		1.7	N/A	N/A
10		105		1.75	N/A	1.77
11			50	1.2	N/A	N/A
12			65	1.38	N/A	N/A
13			90	1.62	N/A	N/A
14			100	1.71	N/A	1.72
15			105	1.75	N/A	1.77

Inverter#1,100% Penetration, 1.71 PU



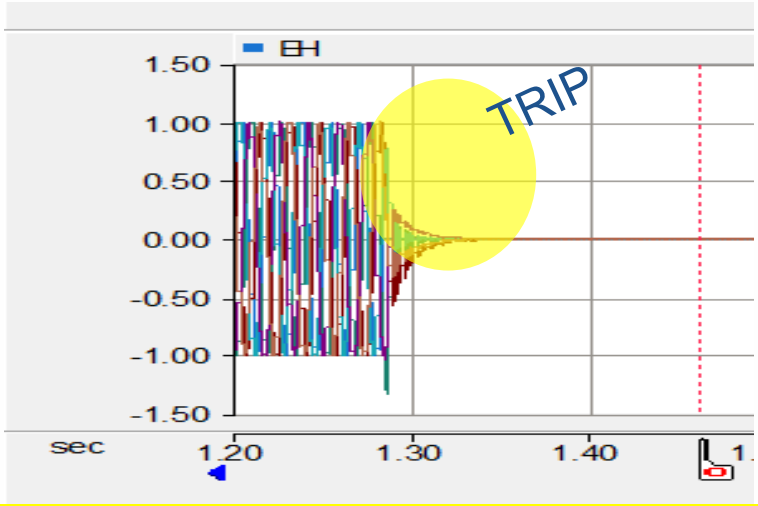
Inverter#1 cannot detect the fault for all scenarios

Inverter#3,100% Penetration, 1.73 PU



Inverter#3 cannot detect the fault for 100 % Penetration Scenario

Inverter#2,100% Penetration, Trip Inst.No overvoltage



Inverter#2 trips for all scenarios

- **Inverter 1 & 3 do not trip and contribute to GFOV**
- **Inverter 2 trips for all scenarios and does not cause GFOV**

Simulation Results

- **Group 2 / Table 3-2 (Scenario 16 through 23).** The objective of the scenarios in this group is to study the impact of the surge arresters in relation to the GFOV as well as to demonstrate the capability of the surge arresters in handling the GFOV

- Surge arresters are expected to lower the GFOV magnitude

- Critical penetration level is determined by the capability of the surge arrester in handling the GFOV. It is assumed that surge arresters are coordinated and designed to protect the substation equipment. Surge arresters are assumed to be the weakest link and will get damaged first for transient and temporary overvoltage

- The Impact of Surge Arresters depends on the type and rating of the arresters. In this study we use 22 kV MCOV, 24.4 kV MCOV, and 29 kV MCOV station class EVP arresters

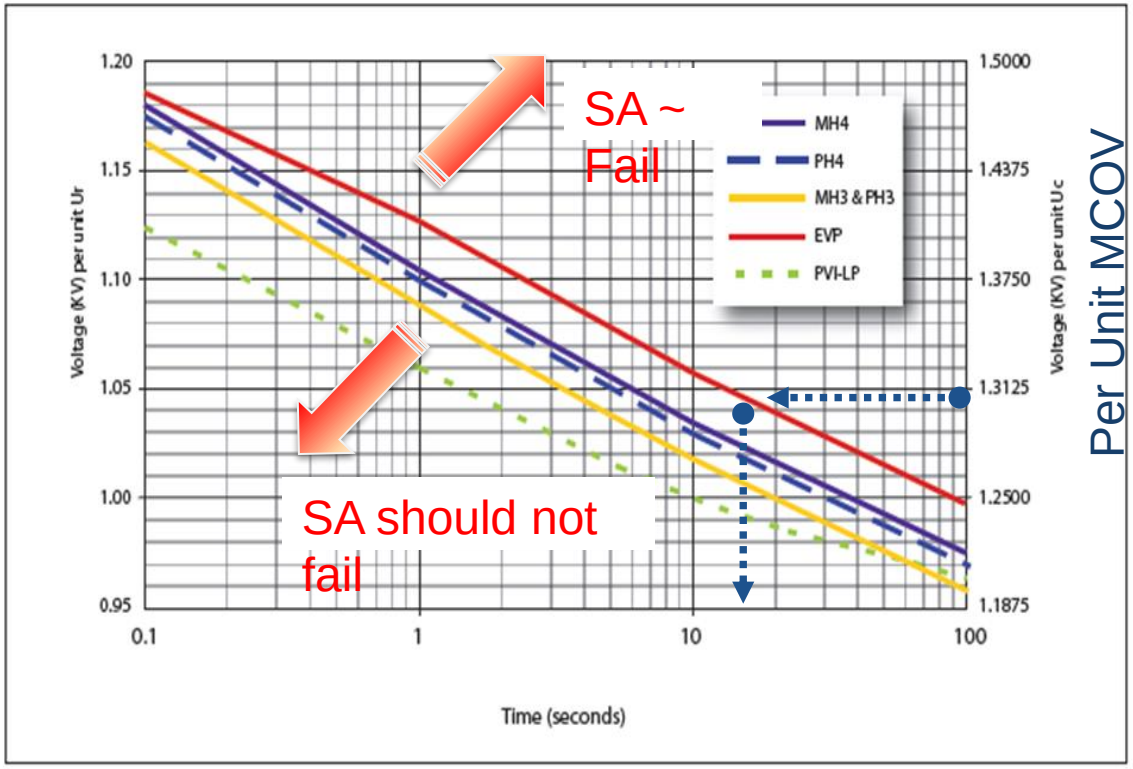
Simulation Results

Scenario	DG/LD_L	DG/LD_H	Temporary Over Voltage						
			Without Surge Arrester PU[1]	22 KV MCOV		24.4 KV MCOV		29 KV MCOV	
				PU	PU of MCOV	PU	PU of MCOV	PU	PU of MCOV
16	65		1.38	1.38	1.25	1.38	1.13	1.38	0.95
17	90		1.62	1.44	1.30	1.56	1.27	1.62	1.11
18	100		1.71	1.45	1.31	1.58	1.29	1.7	1.17
19	105		1.75	1.45	1.31	1.59	1.30	1.75	1.20
20		65	1.38	1.38	1.25	1.38	1.13	1.38	0.95
21		90	1.62	1.44	1.30	1.56	1.27	1.62	1.11
22		100	1.7	1.45	1.31	1.58	1.29	1.7	1.17
23		105	1.75	1.45	1.31	1.59	1.30	1.75	1.20

- 22 kV MCOV and 24.4 kV MCOV reduces GFOV from 1.7 to 1.45 and 1.6
- Consider using arrester's TOV capability – for the criteria. Surge arresters seems not activated for 1.38 PU overvoltage (less likely to get damage at this voltage level).

Simulation Results

	22 KV	24.4 KV	29 KV
PU of MCOV of Surge Arrester Overvoltage for 100% Penetration Level	1.31	1.29	1.17
Time (seconds)	>15	>15	>100



Simulation Results

- **Group 3 / Table 3 (Scenario 24 through 28)** are intended to study the impact of modeling the high-quality load factor and multi inverter cases

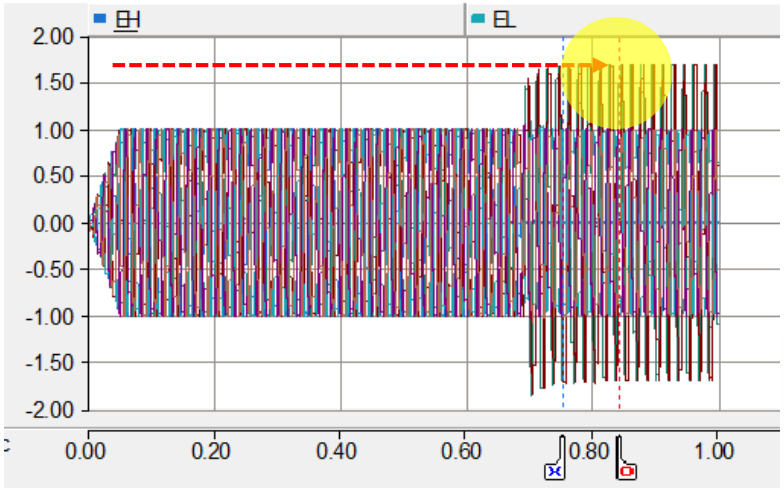
SC	DG/LD_L	Load Quality Factor	Inverters	Over Voltage (Steady State)
24	100	1	Inverter#2	1[2]
25	100	2.5	Inverter#2	1[2]
26	100	N/A[1]	Inverter#1 + Inverter#2	1.2[3]
27	100	1	Inverter#1 + Inverter#2	1.18[3]
28	100	2.5	Inverter#1 + Inverter#2	1.11[3]

$$Q = \frac{\sqrt{Q_L \times Q_C}}{P_R}$$

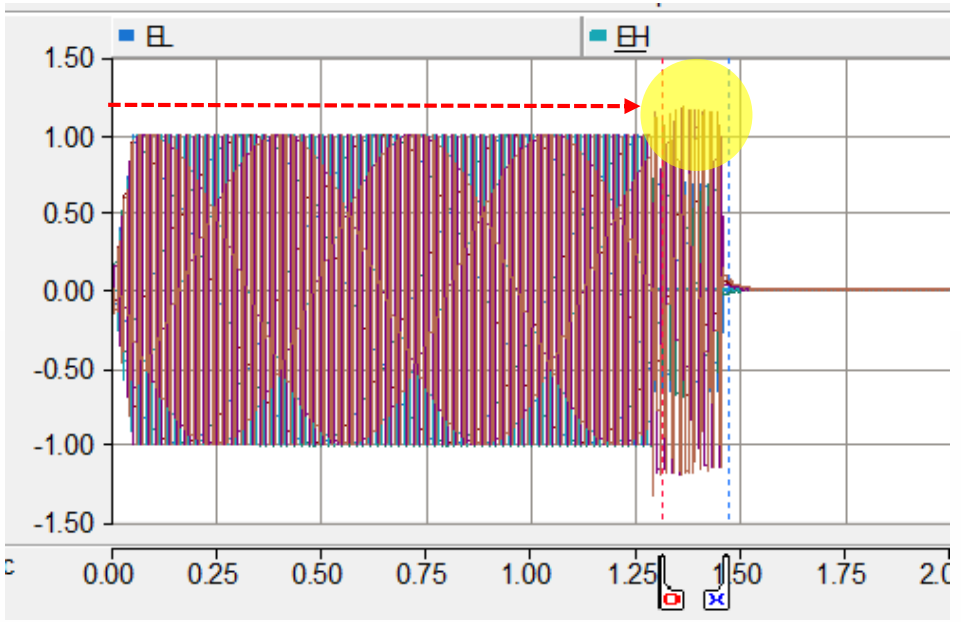
Where:
Q= Load's quality factor
Q_L: Inductive power of the load
Q_C: Capacitive power of the load
P_R: Resistive power of the load

IEEE P1547.1 and IEEE Std.929, respectively, recommended islanding test procedure based on load quality factors of 1 and 2.5.

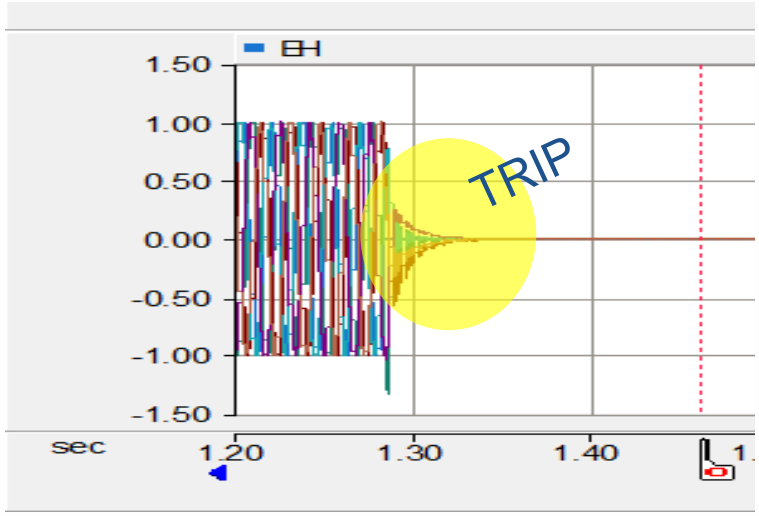
Inverter#1,100% Penetration, 1.71 PU

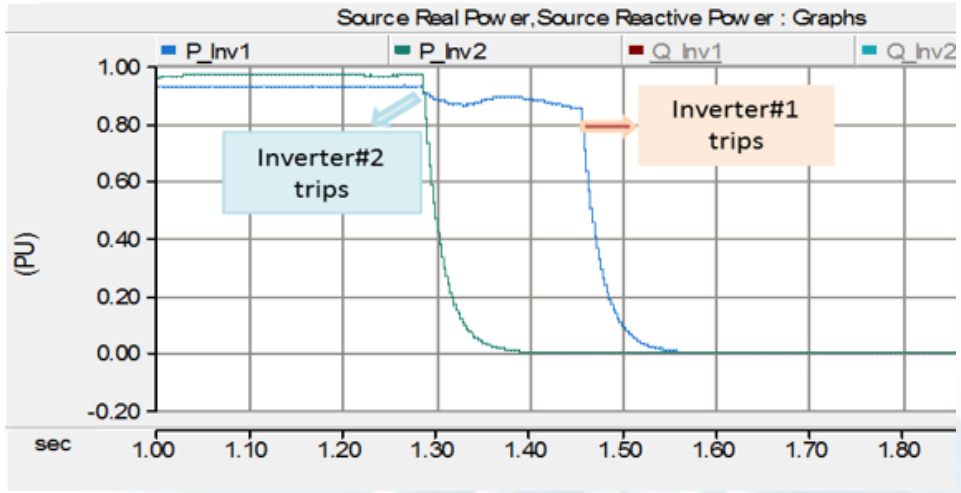


Inverter#1 & 2,100% Penetration, 1.2 PU



Inverter#2,100% Penetration, Trip Inst.,



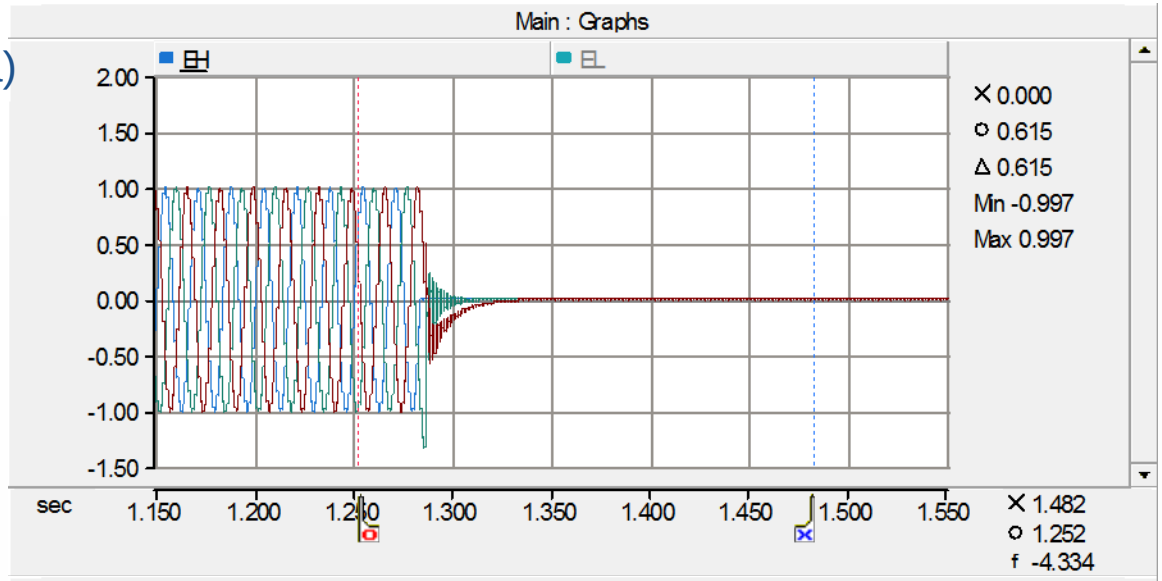


- Multiple inverters on an island does not degrade inverter protection performance
- Inverter #2 still can detect the fault in multiple inverter cases, Inverter#1 trips due to power unbalance (low frequency)

a) Inverter#2,100% Penetration, No load quality factor

b) Inverter#2,100% Penetration, quality load factor = 2.5

a)



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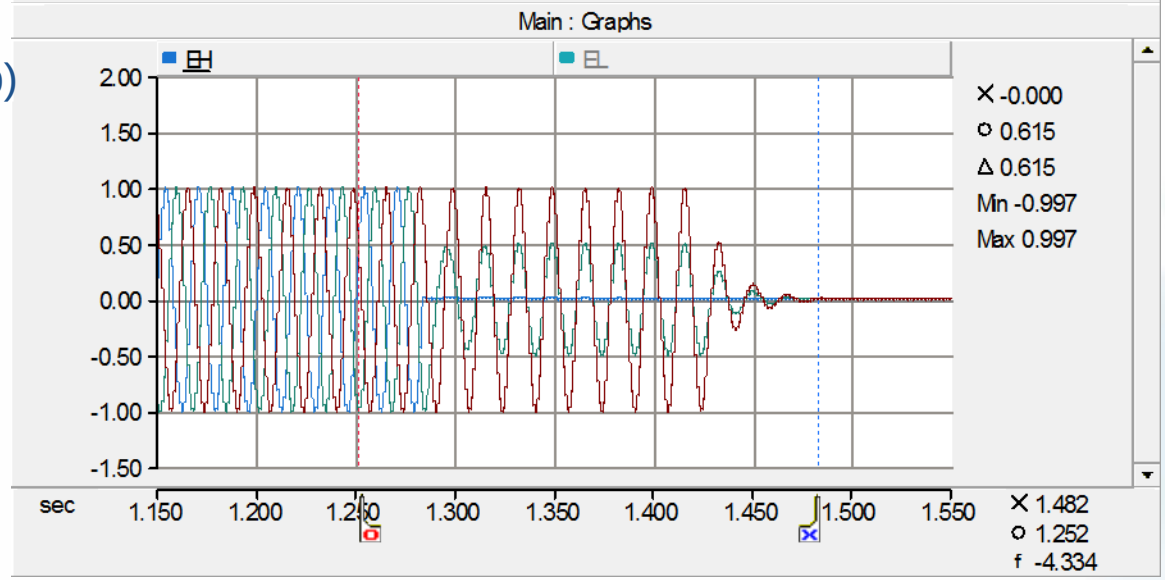

- Higher load quality factor does not change the conclusion of the analysis in terms of potential overvoltage magnitude

Conclusions

- Scenarios in Group 1:
  - Magnitude of overvoltage depends on
    - Inverter type (whether it can detect the fault or not)
    - Penetration level on the island
  - All the load in the island should be included for the GFOV assessment, including subtranmission load
- Scenarios in Group 2:
  - Including surge arrester in the model could reduce TOV
  - Depending on the surge arrester used in the system, a penetration level of 100% is possible assuming arresters are properly coordinated and designed to protect substation equipment
- Scenarios in Group 3:
  - Multiple inverters on an island does not degrade inverter protection performance
  - Modelling higher load quality factor does not change the conclusion of the analysis in terms of potential overvoltage magnitude