Pterra Consulting

Pterra Report R149-16

Assessment of Inverter-based Distributed Generation Induced Ground Fault Overvoltage on Delta-Wye Substation Transformers

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NYSERDA

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Contents

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Executive Summary

New York State Energy Research and Development Authority (NYSERDA) contracted Pterra, LLC ("Pterra") to conduct an engineering study on the conditions when potential ground-fault-overvoltage (GFOV) and a consequent 3V0[1] requirement occurs involving inverter-based distributed generation (DG).

Recent interconnection studies for proposed inverter-based photovoltaic DG have identified a potential regarding GFOV where a portion of the combined subtransmission and distribution system would not have a grounding source after the opening of a recloser or a circuit breaker upstream of the fault location. Such studies, conducted by utilities in New York State, have identified the need for 3VO-based protection schemes to mitigate the potential GFOV. The 3VO requirement could be cost prohibitive for DG projects because it requires installation of new potential transformer (PT) on the transmission side and additional detection and relaying equipment.

The objective of this study was to demonstrate the impact of GFOV with inverter-based distributed generations on a distribution circuit considering the following parameters:

- Penetration level (DG to load ratio) on the islanded system
- The load on distribution, transmission, and combination of both
- Inverter control designs from different manufacturers
- Surge arresters on the transmission side
- The load's Quality Factor

Based on the study, the hope is that a better understanding of the phenomena relating to GFOV and related 3V0 protection is achieved, and alternative potential resolutions that are less cost prohibitive may be identified.

This study is Phase 1 of an ongoing effort to provide technical clarity on the issue of GFOV. This phase is focused on identifying, quantifying and evaluating the potential impacts of the phenomenon of GFOV. Subsequent phases are planned to consider alternative mitigation options and system performance criteria.

This study used time-domain simulation of various operating scenarios to evaluate and clarify the GFOV phenomenon. The software used was the

[1] Normally, the three winding voltages of a transformer add vectorially to zero. When ground faults occur, the voltage that appears corresponds to 3 times the zero-phase-sequence component of any one of the three phase-to-ground voltages at the potential-device location. This voltage is referred to as "3V0 " and is the basis for certain types of protective relaying schemes.

PSCAD/EMTDC commercial package developed by the Manitoba HVDC Research Center.

A test system comprising of a subtransmission circuit feeding a distribution feeder through a delta-wye grounded transformer was modeled in software. Proprietary manufacturer models for three different inverter designs were integrated with the model. Twenty-eight scenarios were then developed to help focus on various aspects of GFOV. These scenarios can be generally grouped into the following:

- Scenarios to identify critical penetration levels for different inverters, load locations, and DG to load ratio
- Scenarios illustrating the effect of surge arresters in the simulations
- Scenarios to evaluate the impact of multiple inverters of different manufacture
- Scenarios to study the impact of load quality factor

FINDINGS:

The following is a summary of the findings of this study based on the observed results of simulations.

- While inverters can potentially cause overvoltage on the delta side of the substation transformer, some inverter designs can detect a single-line-to-ground fault condition and trip instantaneously. Time domain simulation is a potential tool for evaluating the fault detection capability of inverters for this purpose.
- According to ANSI/IEEE C62.92, the GFOV for an effectively grounded system is to be limited to 138%. This value can also be used to limit the overvoltage for ungrounded systems. Simulation results indicate that overvoltage on the delta side of the study substation transformer peaks at 1.38 PU as the PV/load ratio approaches 65%. At penetration levels below 65%, no overvoltage is observed. Two important notes relate to this finding:
    a. The calculation for the load should account for those connected to the transmission side as well as the distribution side of the isolated system.
    b. Though this ratio seems close to the threshold proposed by National Grid (i.e. 67%), there is possibility of under counting the load if only the distribution side load is considered.
- The 65% penetration limit (based on 1.38 PU overvoltage threshold) can be relaxed if:

a. Damage to equipment connected to delta side of the substation transformer is the reason for requiring 3VO protection; and

b. Surge arresters connected to delta side of the substation transformer are taken into account

Simulations conducted in this study with station class surge arresters indicate that arresters can safely operate for penetration levels of up to 100%.

This report is not intended to impose pass-fail criteria for GFOV nor does it provide basis for requiring 3VO protection due to GFOV. The intention is to add to the body of knowledge on this topic and contribute to future pass-fail criteria that may be developed through a consensus-based process including various industry stakeholders and taking into account all circuit configurations, a variety of inverter manufacturers and the best available information on distribution system requirements.

FUTURE WORK:

As noted earlier, this study is phase 1 of an overall effort to provide technical clarity on the issue of GFOV. A future aspect of study is:

- Investigation of less expensive countermeasures for 3V0 requirement to alleviate a potential GFOV issue. Such countermeasures could include, but not limited to, protective relaying detection on the distribution side, detection by the inverter, application of a grounding switch on distribution feeder, and addition of a grounding bank on the transmission side.

Section 1. Introduction

New York State Energy Research and Development Authority (NYSERDA) contracted Pterra, LLC ("Pterra") to conduct the following engineering study in relation to ground-fault-overvoltage (GFOV) impact and mitigation via 3VO protection.

1.1. Background of 3V0 Requirements

Recent interconnection studies for proposed inverter-based photovoltaic DG have identified a potential regarding GFOV where a portion of the combined subtransmission and distribution system would not have a grounding source after the opening of a recloser or a circuit breaker upstream of the fault location. Such studies, conducted by utilities in New York State, have identified the need for 3VO-based protection schemes to mitigate the potential GFOV. The present 3VO requirement could be cost prohibitive for DG projects because it requires detection and installation of potential transformers (PT) on the transmission side as shown in Figure 1-1, highlighted in yellow.

To further illustrate the problem related to GFOV and the 3VO protection requirement, the following sequence of events can be postulated:

1. A single-line-to-ground (SLG) fault occurs at any of the locations F1, F2, or F3. For this example, we assume the fault location is at F1 or Phase A as shown in Figure 1-1.
2. The fault is detected by the subtransmission protection which would trip the circuit breaker. Prior to the opening of the circuit breaker, there is no overvoltage because the ground source from sub-transmission system is still intact. Figure 2-2(b) show VAN = 0, VBN = VCN = 1 PU.
3. After several cycles of the SLG fault detection, the circuit breaker trips; At this point the system loses its grounding source and causes neutral point to shift. The overvoltage could occur on the un-faulted phases as shown in Figure 2-2(c): VBN = VCN =1.732 PU or 173% overvoltage, , assuming an initial voltage of 1.0 PU.
4. One option to protect against the overvoltage is to provide for 3V0 detection capability through the installation of PTs on the high-side of the transformer and consequent tripping signals.

A key assumption that supports this sequence of events is:

- DG does not detect the fault and does not trip immediately and thus continue to energize and feed the fault.

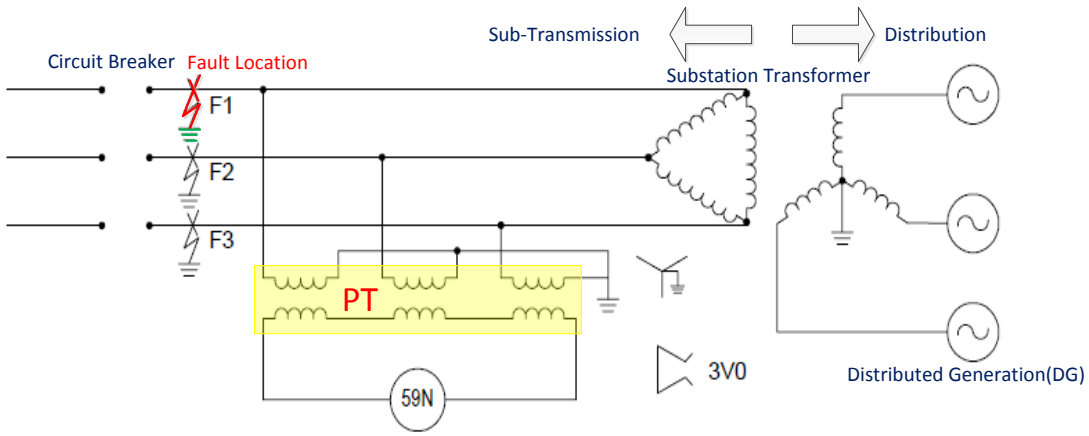


Figure 1-1. Illustration of the 3VO Requirement with Potential Transformer (PT) on the Transmission Side

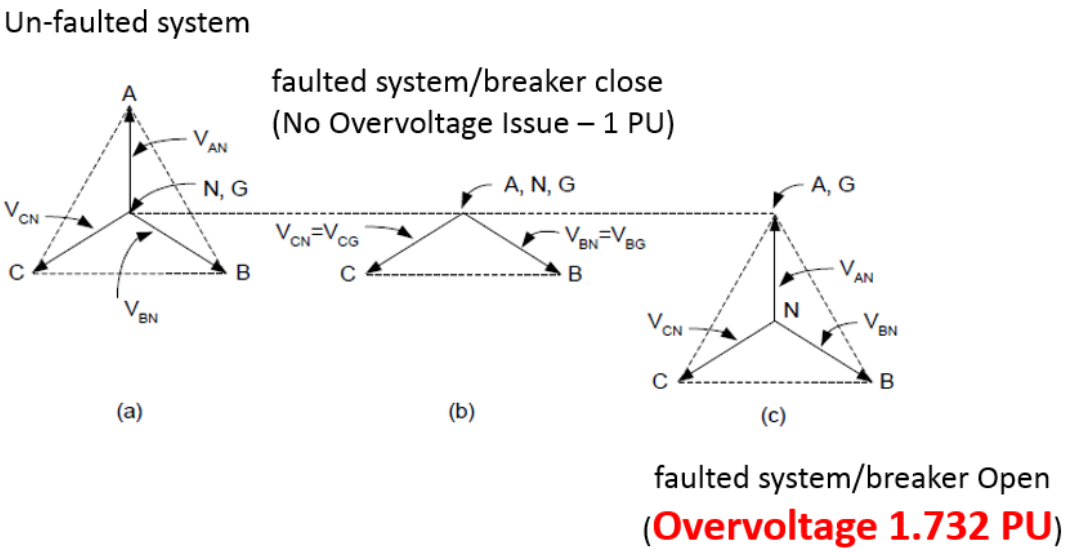


Figure 1-2. (a)Voltages Prior to Single-line-to-ground Fault (SLG), (b)During SLG with Breaker Close, and (c)During SLG with Breaker Open

1.2. Objective

The objective of this study is to demonstrate the impact of GFOV with inverter-based distributed generations on a distribution circuit considering the following parameters:

- Penetration level (DG to load ratio) on the islanded system
- The load on distribution, transmission, and combination of both
- Inverter control designs from different manufacturers
- Surge arresters on the transmission side
- The load's Quality Factor

Section 2. Methodology and Assumptions

2.1. Methodology

Time domain simulation software (PSCAD™)[2] is used for the assessment. Figure 2-1 shows a test circuit considered in this report for evaluation of ground fault overvoltage in an islanded circuit. After DG (i.e. PV) reaches steady state condition, a permanent single line to ground fault is initiated on delta side of substation transformer. In five cycles, circuit breaker connected on faulted side of transformer opens to clear the fault from the grid. The operation of the circuit breaker forms an island with local loads and existing PVs. Single line to ground fault together with the lack of grounding source makes delta side of transformer vulnerable to high overvoltage.

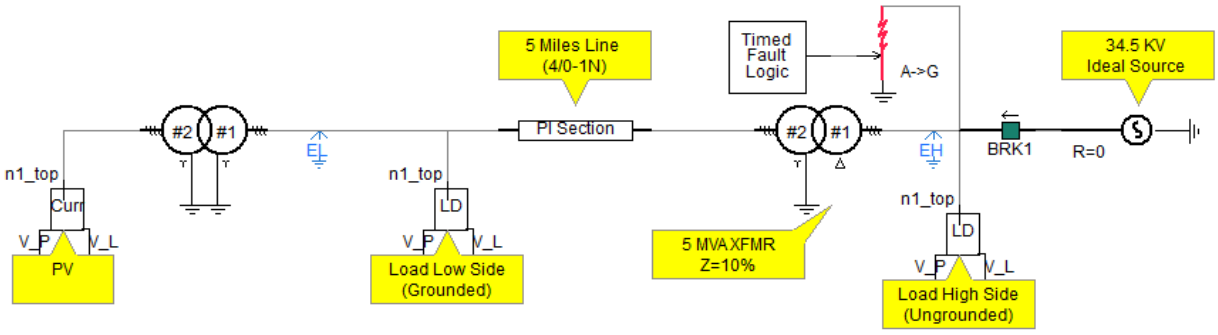


Figure 2-1: Single Line Diagram of Studied Circuit with Single Inverter

A total of 28 Scenarios were identified, developed and tested for the study. The scenarios are summarized in three tables, as follows:

1. **Table 3-1 (Scenario 1 through 15)**. The objective of these scenarios is to illustrate critical penetration level for different inverters, load locations, and DG to load ratio.

   Three inverters used for the study are commercially available; however, manufacturer names and model numbers are replaced using arbitrary designations for confidentiality.

   - Inverter#1: 250 kW, three-phase, UL-1741 certified
   - Inverter#2: 250 KW, three-phase, UL-1741 certified
   - Inverter#3: 1 MW, three-phase, UL-1741 certified

[2] PSCAD/EMTDC is a commercial software package developed by the Manitoba HVDC Research Center.

Three locations of the load were considered:

- All the load is on the transmission side/delta side of the substation transformer. Load on delta side is assumed un-grounded.
- All the load is on the distribution side / wye-grounded side of the substation transformer. Load on wye side is assumed grounded.
- Combination of the above

For each inverter, the load on the circuit was modified in such a way that the DG to load ratio (penetration level) in the island varies from 50% to 105%.

Critical penetration level is then determined when the GFOV reaches the magnitude of 1.38 PU. According to ANSI/IEEE C62.92, the GFOV for an effectively grounded system is limited to 138%. In other words, even if there is no DG on the circuit, the 138% GFOV still could be expected on an effectively grounded system.

2. **Table 3-2 (Scenario 16 through 23).** The objective of these scenarios is to study the impact of the surge arresters in relation to the GFOV as well as to demonstrate the capability of the surge arresters in handling the GFOV.

   Critical penetration level is determined by the capability of the surge arrester in handling the GFOV. It is assumed that surge arresters are coordinated and designed to protect the substation equipment.

3. **Table 3-3 (Scenario 24 through 28)** are intended to study the impact of multiple inverter-types connected to the same feeder and modeling of high-quality load factors.

2.2. Assumptions

The following assumptions apply to the modeling of scenarios and the simulations conducted:

- To obtain conservative results, active anti-islanding protections in inverters and non-linearity of transformers (magnetizing and saturation) were deactivated in all scenarios.
- The external grid is modeled as an ideal source. This assumption also leads to conservative results as infinite short circuit capability of the grid tends to mask the fault for inverters.
- The reactive portion of the load is tuned to minimize reactive power mismatch in the island. This is likewise a conservative assumption. Note that Pterra has studied many inverter models developed by leading vendors. A common pattern observed in all studied models indicates that even small amount reactive power mismatch is sufficient for such inverters to detect islanding conditions.
- The current chopping limit for the circuit breaker is at zero amps.

Section 3. Simulation Results and Discussion

For clarity, simulation results are presented and discussed based on the group of scenarios as summarized in Table 3-1, Table 3-2, and Table 3-3. All the simulation plots are provided in Appendix 1.

3.1. Scenario 1 through 15 (Table 3-1)

The objective of these scenarios is to illustrate critical penetration level for different inverters, load locations, and DG to load ratio.

Table 3-1 summarizes the first set of simulation results. This table shows the GFOV magnitude on the delta side of the substation transformer. It is observed that GFOV depends on penetration level and individual inverter's control and protection scheme. Table 3-1 also shows that the load on sub-transmission side or delta side of substation transformer will affect the magnitude of the GFOV and should be considered in the GFOV study.

The loads are modeled as follows:

- In Scenario #1 through #5, the load is connected on wye side or distribution side of the substation transformer. The penetration level is varied from 50% to 105%.
- Scenario# 6 through 10 are similar Scenario #1 through #5, except the load is connected on delta side or sub-transmission side of the substation transformer.
- Scenario 11 through 15 are similar to Scenario#1 through #5, except the loads are connected to both distribution and sub-transmission side.

Each scenario was simulated with each of three different inverters mentioned in Section 2. Since inverters have different initialization time, fault initialization time was different among studied cases. The fault was activated at .6 s, 1.2 s and 1.6 s for Inverter#1, Inverter #2, and Inverter #3, respectively. In all cases, circuit breaker *BRK1* in Figure 2-1 clears the fault from the grid in five cycles.

From the simulation plots, Inverter#1 did not detect the fault and maintained energization of the island for all scenarios. Inverter#2 detects the fault and trips within 3 cycles after the island is formed in all scenarios. The fault detection performance for Inverter#3 falls between Inverter #2 and Inverter #1.

Among the three inverters, the inverter with the least fault detection capability (i.e. inverter#1) first caused GFOV of 1.38 PU on the delta side of substation transformer when penetration level increased to 65%. According to ANSI/IEEE C62.92, the GFOV for an effectively grounded system is limited to 138%. Assuming 1.38 PU as the maximum permissible overvoltage for the GFOV, the critical penetration limit is 65%. This penetration limit is slightly lower than the 67% criteria used by a National Grid.

It should be noted that loads connected to delta side or sub-transmission system should be considered in the calculation of the penetration level. Comparison among scenario#1 through scenario#5, scenario#6 through scenario#10 and scenario# 11 through scenario#15 show comparable GFOV magnitude for the cases with different load locations.

Table 3-1: Scenarios without Surge Arresters

Scenario	DG/LD_L[1] %	DG/LD_H[2] %	DG/(LD_L+LD_H) %	Over Voltage (Steady State)		
				Inverter#1	Inverter#2	(Inverter#3)
1	50			1.2	N/A[3]	N/A
2	65			1.38	N/A	N/A
3	90			1.62	N/A	N/A
4	100			1.71	N/A	1.73
5	105			1.75	N/A	1.78
6		50		1.2	N/A	N/A
7		65		1.38	N/A	N/A
8		90		1.62	N/A	N/A
9		100		1.7	N/A	N/A
10		105		1.75	N/A	1.77
11			50	1.2	N/A	N/A
12			65	1.38	N/A	N/A
13			90	1.62	N/A	N/A
14			100	1.71	N/A	1.72
15			105	1.75	N/A	1.77

1) LD_L load on the distribution side / low voltage or wye-grounded side of the substation transformer
2) LD_H load on the sub-transmission side / high voltage or delta side of the substation transformer
3) N/A: No overvoltage was observed. Inverter tripped almost instantaneously following fault/islanding

3.2. Scenario 16 through 23 (Table 3-2)

Overvoltage magnitudes tabulated in Table 3-1 can be conservative because no surge arresters were considered for the substation transformer. Potential overvoltage can be further reduced by considering the effect of surge arresters.

The impact of surge arresters depends on the type and rating of the arresters. In order to illustrate the impact of surge arresters, selected scenarios in Table 3-1 were repeated with the following surge arresters:

- Case A: One 22 KV MCOV station class surge arrester (i.e. EVP0 02200) on transmission side
- Case B: One 24.4 KV MCOV station class surge arrester (i.e. EVP0 02400) on transmission side
- Case C: One 29 KV MCOV station class surge arrester (i.e. EVP0 02400) on transmission side

Simulation results are tabulated in Table 3-2. In scenario 16 through scenario#19, the load is connected to distribution feeder; whereas in scenario#20 through scenario#23, the load is connected to the transmission (delta side of the transformer).

Simulation results tabulated in Table 3-2 demonstrate the importance of surge arrester rating, as follows:

- In Case A, the 22 KV MCOV surge arrester limits the overvoltage to 1.45 PU for all considered penetration levels as compared to 1.75 PU in the case without surge arrester.
- In Case B, the 24.4 KV MCOV surge arrester limits the overvoltage to 1.6 PU for all considered penetration levels as compared to 1.75 PU in the case without surge arrester.
- In Case C, the 29 KV MCOV surge arrester does not have a noticeable impact on the overvoltage level because the overvoltage as compared to its MCOV rating is not high enough to activate the surge arrester to absorb the temporary overvoltage.

Table 2: Scenarios with Surge Arresters-Inverter#1

Scenario	DG/LD_L	DG/LD_H	Temporary Over Voltage						
			Without Surge Arrester PU[1]	22 KV MCOV		24.4 KV MCOV		29 KV MCOV	
				PU	PU of MCOV	PU	PU of MCOV	PU	PU of MCOV
16	65		1.38	1.38	1.25	1.38	1.13	1.38	0.95
17	90		1.62	1.44	1.30	1.56	1.27	1.62	1.11
18	100		1.71	1.45	1.31	1.58	1.29	1.7	1.17
19	105		1.75	1.45	1.31	1.59	1.30	1.75	1.20
20		65	1.38	1.38	1.25	1.38	1.13	1.38	0.95
21		90	1.62	1.44	1.30	1.56	1.27	1.62	1.11
22		100	1.7	1.45	1.31	1.58	1.29	1.7	1.17
23		105	1.75	1.45	1.31	1.59	1.30	1.75	1.20

1) Results from Table 3-1, it is included in this table for comparison purpose

Table 3-1 considers 1.38 PU as the maximum permissible overvoltage on high voltage side of the substation transformer. Using the same criteria, Table 2 shows the GFOV of 1.38 PU occurs when penetration level reaches 65%. This is the same PV penetration limit found in scenarios without surge arresters (See Table 3-1). Table 2 shows the surge arresters start making a difference in reducing the overvoltage when the overvoltage is higher than 1.38 PU.

Assuming surge arresters are designed to protect the substation equipment, they should be the first component on the substation to get damaged due to overvoltage conditions. Figure 3-1 shows temporary overvoltage capability of EVP surge arresters used in Case A, B, and C. Comparing the overvoltage levels summarized in Table 2 with the curve shown in Figure 3-1, the following can be observed:

- 22 KV MCOV and 24.4 KV MCOV surge arresters can safely operate for up to 15 seconds even when penetration level is 105%.
- With the same penetration level, 29 KV MCOV arrester can operate for more than 100 seconds.

In the absence of rotating generators, it is extremely unlikely to have run-on islanding time in the order of 15 seconds. Thus, considering the surge arresters used in this study, the critical penetration limit could be set at 100%.

Note that TOV capability curve of surge arresters connected to delta side of a substation transformer is needed prior to determining penetration limit based on equipment damage. Simulations conducted in this study with station class surge arresters indicate that arresters can safely operate for penetration level as high as 100%.

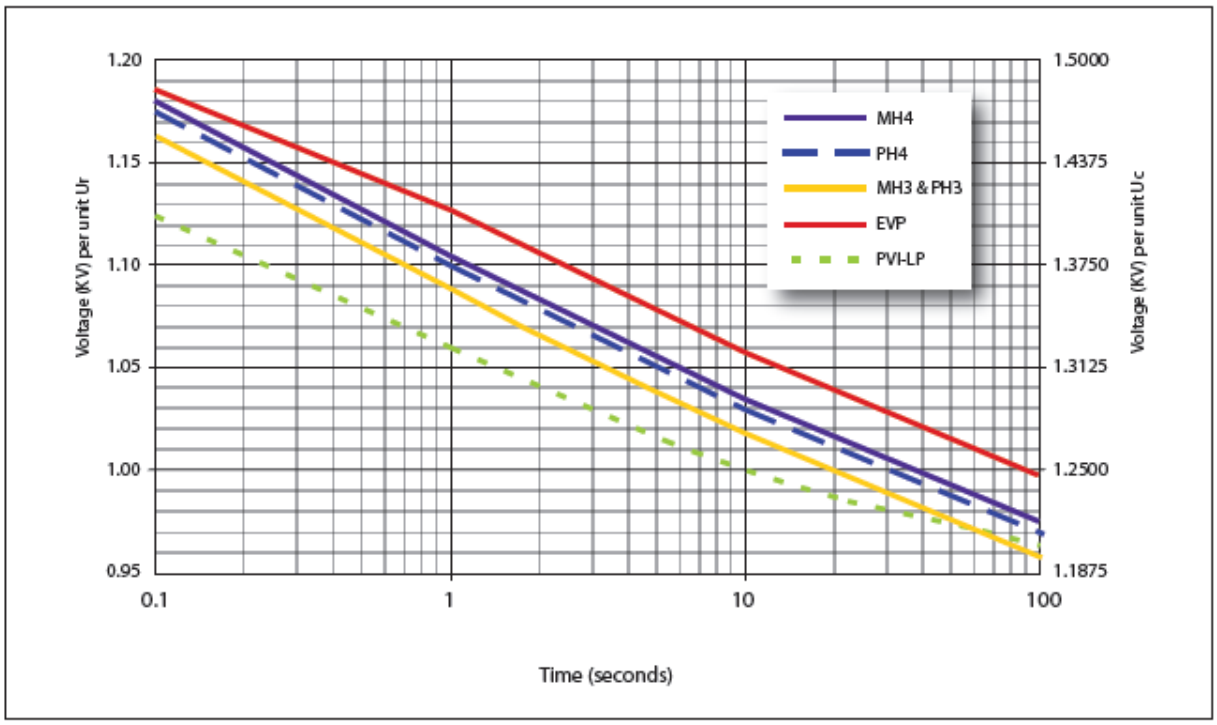


Figure 3-1: Temporary Overvoltage Capability of EVP Surge Arresters with Prior Duty

3.3. Scenario 24 through 28 (Table 3-3)

These scenarios are intended to study multi-inverter cases as well as potential impacts of having a load with a high-quality factor.

The quality factor of the load can be defined as:

$$Q = \frac{\sqrt{Q_L \times Q_C}}{P_R}$$

Where:
Q= Load's quality factor
Q_L: Inductive power of the load
Q_C: Capacitive power of the load
P_R: Resistive power of the load

It is generally more difficult to detect islanding condition when islanded load has a high-quality factor and resonates close to the fundamental frequency. IEEE P1547.1 and IEEE Std.929, respectively, recommended islanding test procedure based on load quality factors of unity and 2.5. The test requirement of Q<2.5 has been determined to cover all reasonable distribution line configurations.

Table 3-3 summarizes the simulation results which demonstrate the following:

- Although the high value of the Q indicated the potential impact on islanding duration, changing load's quality factor in studied scenarios does not change the conclusion of the analysis in terms of potential overvoltage magnitude at high voltage side of substation transformer.
- Having multiple inverters on an island does not necessarily degrade protection performance of inverters from GFOV point of view.

The scenarios in Table 3-3 consider PV penetration fixed at 100% and the load was assumed to be connected to low voltage side of the substation transformer (wye side).

Scenario #24 and 25 were considered to evaluate load's quality factor in the single-inverter case. Inverter#2 was chosen for these scenarios because it was the only inverter which tripped for 100% penetration in scenario#4, 9 and 14 (i.e. cases without high-quality factor load).

Scenario#26 considered a multi-inverter case composed of inverter#1 and inverter#2. The impact of load's quality factor in the multi-inverter case was illustrated in scenario #27 and #28. Maximum overvoltage observed in scenario#26, #27 and #28 at high voltage side of the substation transformer is about 1.2 PU.

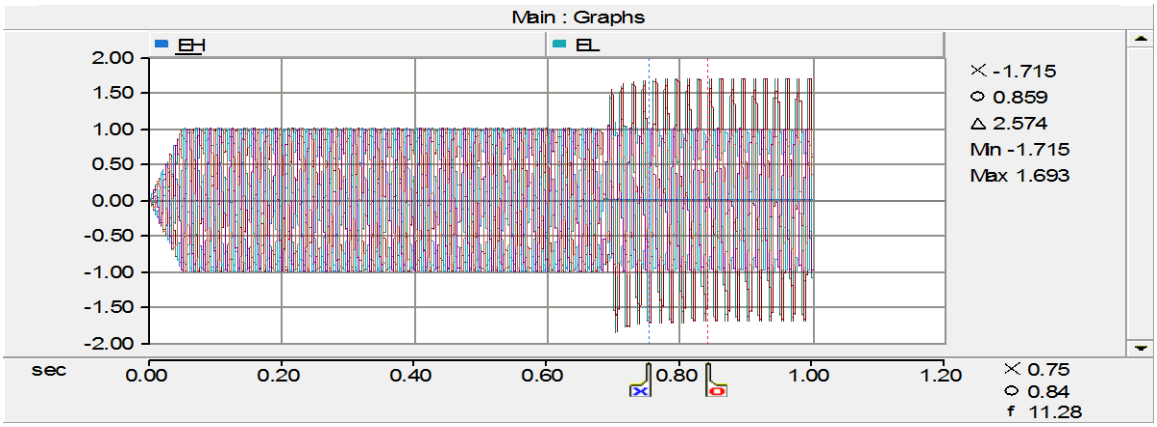
Figure 3-2(a),3-2(b), and 3-2(c), respectively, show voltage at high voltage side of substation transformer in scenario#4 with Inverter#1, scenario#4 with Inverter#2 and scenario#26 (both Inverter#1 and 2). Figure 3-3 plots outputs of both inverters power output of scenario#26. Figure 3-2 and Figure 3-3 illustrate that having multiple inverters on an island does not necessarily degrade protection performance of inverters.

For scenarios in this assessment, overvoltage observed in scenario#26 with both of inverter#1 and inverter#2 is much lower than overvoltage in scenario#4 with inverter#1 only. If one of the inverters in the island can detect abnormal situation and trip, island's operating point drifts from balanced power zone, which in turn, help other inverters to detect abnormality/islanding condition and expedite collapse of the island. In addition, trip of one of the inverters reduce the ratio of in service DG over the load; therefore, reduce potential overvoltage on delta side of the transformer. The worst case is expected when none of the inverters can detect the fault and subsequent islanding condition. Such a case is essentially similar to have an island composed of a single type of inverter with ineffective protection scheme. In this case, penetration level may need to be limited to 65% or 100% depending on consideration of the surge arrester capability in handling the overvoltage before 3V0 or other protection is considered.

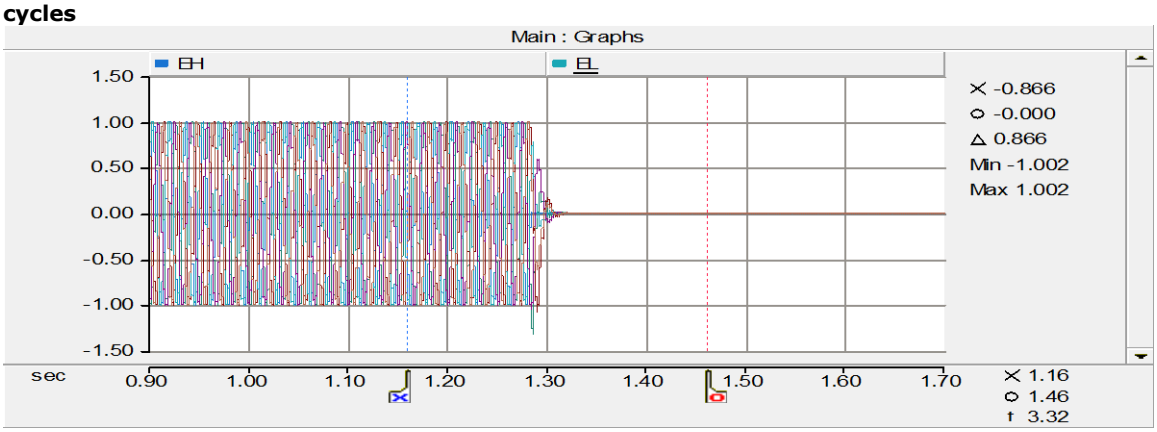
Table 3-3: Scenarios with High-Quality Factor Load/Multi-Inverters

SC	DG/LD_L	Load Quality Factor	Inverters	Over Voltage (Steady State)
24	100	1	Inverter#2	1[2]
25	100	2.5	Inverter#2	1[2]
26	100	N/A[1]	Inverter#1 + Inverter#2	1.2[3]
27	100	1	Inverter#1 + Inverter#2	1.18[3]
28	100	2.5	Inverter#1 + Inverter#2	1.11[3]

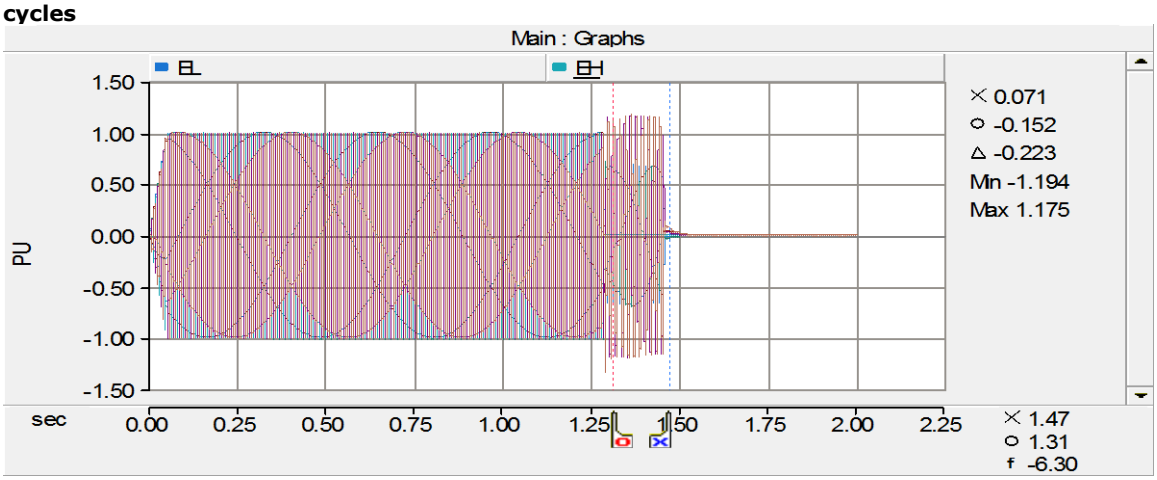
1) Load with high-quality factor is not in service in scenario#26. The load is modeled similar to scenarios in Table 3-1 or Scenario 1-15
2) Inverter trip following islanding; No overvoltage was observed.
3) In scenario#26,27 and 28, inverter#2 trip almost instantaneously after islanding. Inverter#1 trip within .6s after inverter#2.



a) Scenario 4 with Inverter#1, Permanent SLG fault initiates at t=.6 s; circuit breaker opens after 5 cycles



b) Scenario 4 with Inverter#2, Permanent SLG fault initiates at t=1.2 s; circuit breaker opens after 5 cycles



c) Scenario 26 with Inverter 1 & 2, Permanent SLG fault initiates at t=1.2 s; circuit breaker opens after 5 cycles

Figure 3-2: Per Unit Voltage at Delta side of Substation Transformer

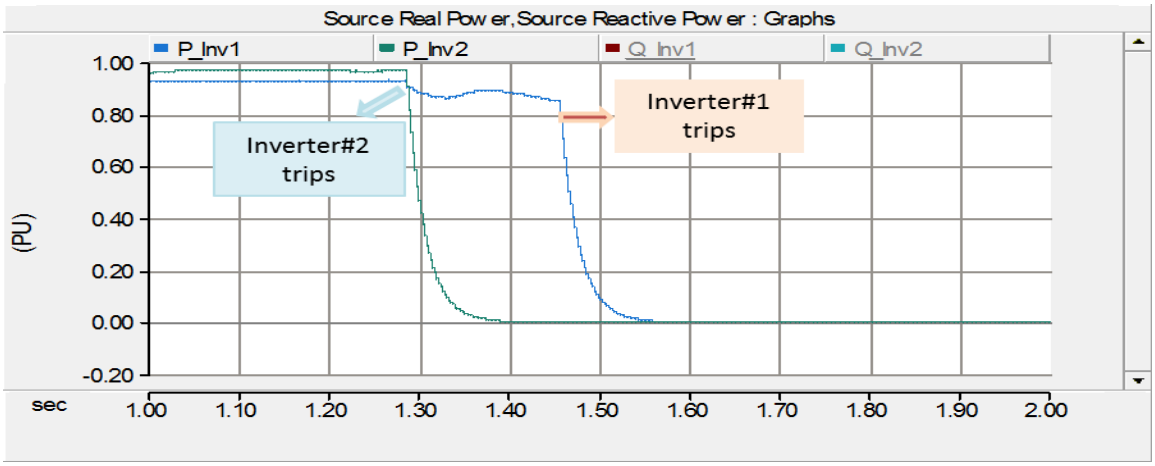


Figure 3-3: Inverter's Output Power in Scenario#26

Figure 3-4 show voltage at high voltage side of substation transformer of scenario#25 where load quality factor is equal to 2.5. Comparison of Figure 3-2(b) (i.e. inverter#2 without high-quality factor load) and Figure 3-4 (i.e. inverter#2 with load quality factor of 2.5) illustrates how load's quality factor can increase islanding duration. In this case, it increases from about 3 cycles to about 12 cycles.

Although the high value of the Q indicated the potential impact on islanding duration, changing load's quality factor in studied scenarios did not change the conclusion of the analysis in terms of potential overvoltage magnitude at high voltage side of substation transformer. In other words, no incremental impact was observed on the magnitude of overvoltage at high voltage side of substation transformer due to load with the high-quality factor. Comparing scenario# 24 and #25 with scenario#4 illustrates that even with the addition of high-quality factor load, inverter#2 is still able to detect the single-line-to-ground fault and trip. Similarly, comparing scenario#27 and #28 with scenario#26 indicates that loads quality factor does not significantly affect the GFOV magnitude in the multiple inverters cases.

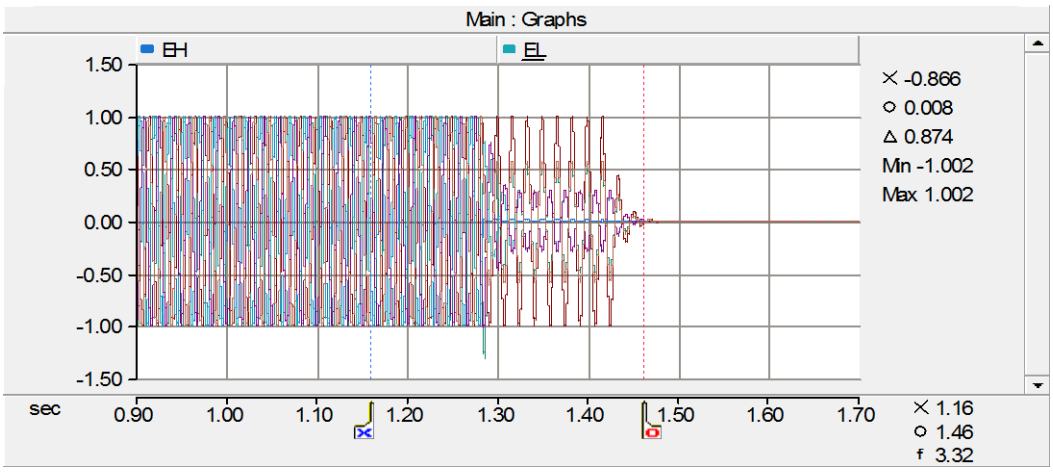


Figure 3-4: Voltage at Delta side of Substation Transformer in Scenario#25

Section 4. Conclusions and Future Work

4.1. Conclusions

Time domain simulations were performed for three commercial inverter models to illustrate potential GFOV on delta side of delta-wye substation transformers due to penetration of inverter based DG on wye side of transformer feeding distribution feeders.

The following is a summary of the findings of this study based on the observed results of simulations.

- While inverters can potentially cause overvoltage on the delta side of the substation transformer, some inverter designs can detect a single-line-to-ground fault condition and trip instantaneously. Time domain simulation is a potential tool for evaluating the fault detection capability of inverters for this purpose.
- According to ANSI/IEEE C62.92, the GFOV for an effectively grounded system is to be limited to 138%. This value can also be used to limit the overvoltage for ungrounded systems. Simulation results indicate that overvoltage on the delta side of the study substation transformer peaks at 1.38 PU as the PV/load ratio approaches 65%. At penetration levels below 65%, no overvoltage is observed. Two important notes relate to this finding:
    a. The calculation for the load should account for those connected to the transmission side as well as the distribution side of the isolated system.
    b. Though this ratio seems close to the threshold proposed by National Grid (i.e. 67%), there is possibility of under counting the load if only the distribution side load is considered.
- The 65% penetration limit (based on 1.38 PU overvoltage threshold) can be relaxed if:
    a. Damage to equipment connected to delta side of the substation transformer is the reason for requiring 3VO protection; and
    b. Surge arresters connected to delta side of the substation transformer are taken into account

    Simulations conducted in this study with station class surge arresters indicate that arresters can safely operate for penetration levels of up to 100%.

This report is not intended to impose pass-fail criteria for GFOV nor does it provide basis for requiring 3VO protection due to GFOV. The intention is to add to the body of knowledge on this topic and contribute to future pass-fail criteria that may be

developed through a consensus-based process including various industry stakeholders and taking into account all circuit configurations, a variety of inverter manufacturers and the best available information on distribution system requirements.

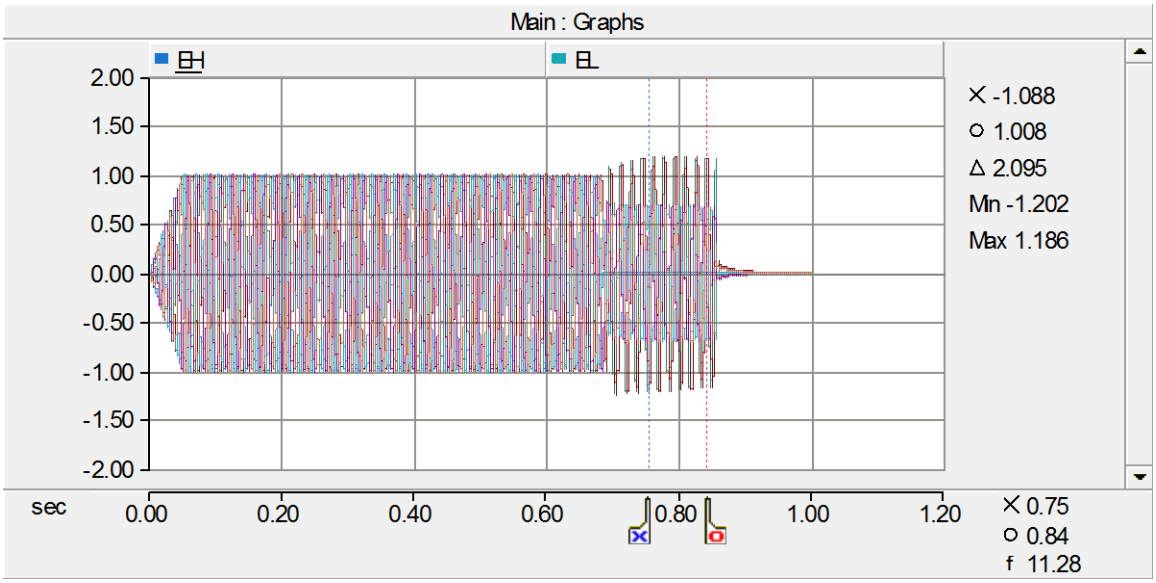
4.2. Future Work

This study is phase 1 of an overall effort to provide technical clarity on the issue of GFOV. A future aspect of study is:

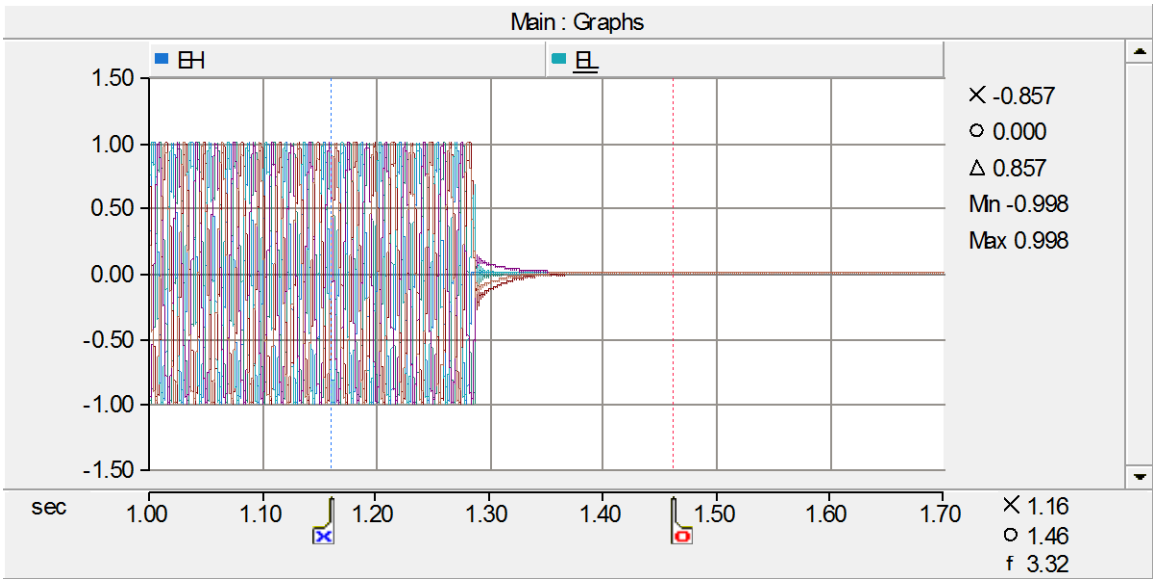
- Investigation of less expensive countermeasures for 3V0 requirement to alleviate a potential GFOV issue. Such countermeasures could include, but not limited to, protective relaying detection on the distribution side, detection by the inverter, application of a grounding switch on distribution feeder, and addition of a grounding bank on the transmission side.

Appendix A-Simulation Plots for Each Scenario

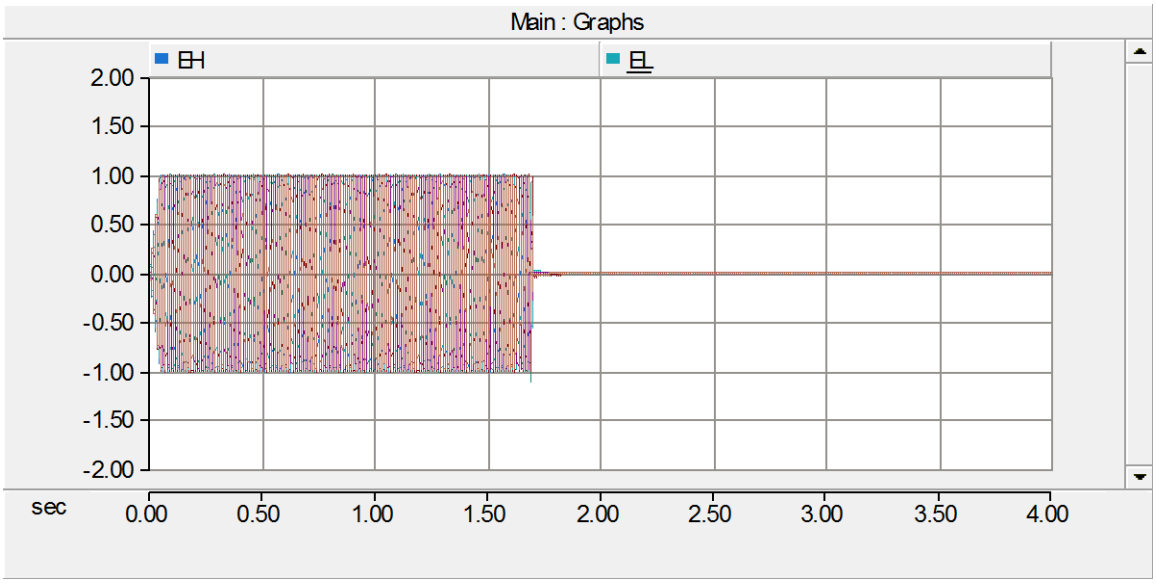
4.2.1. Scenario#1



Delta Side Voltage with INVERTER#1_250 KW

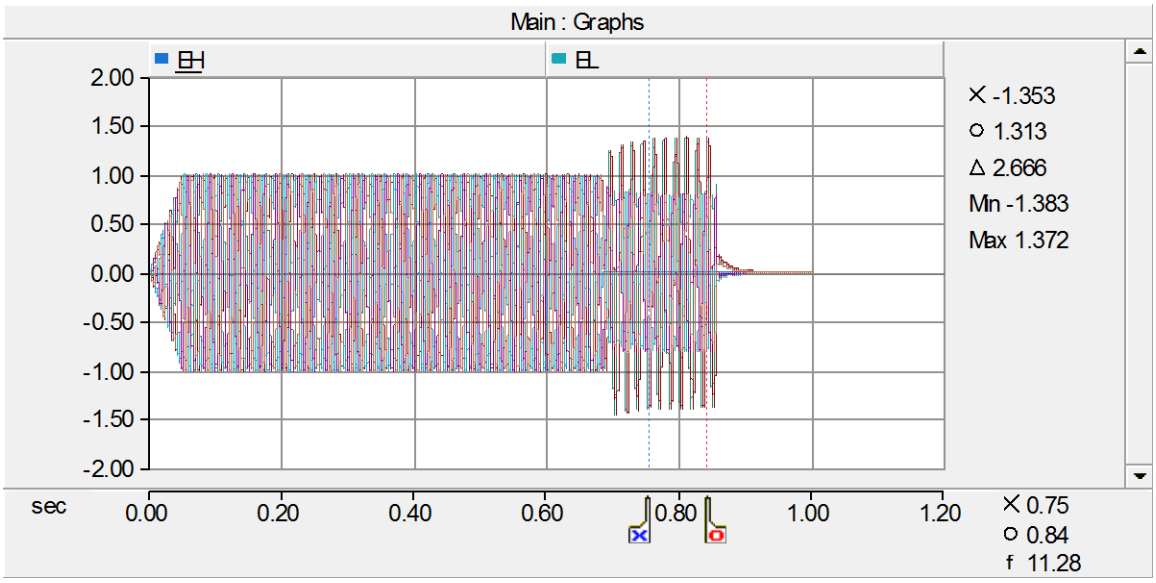


Delta Side Voltage with Inverter#2_250 KW

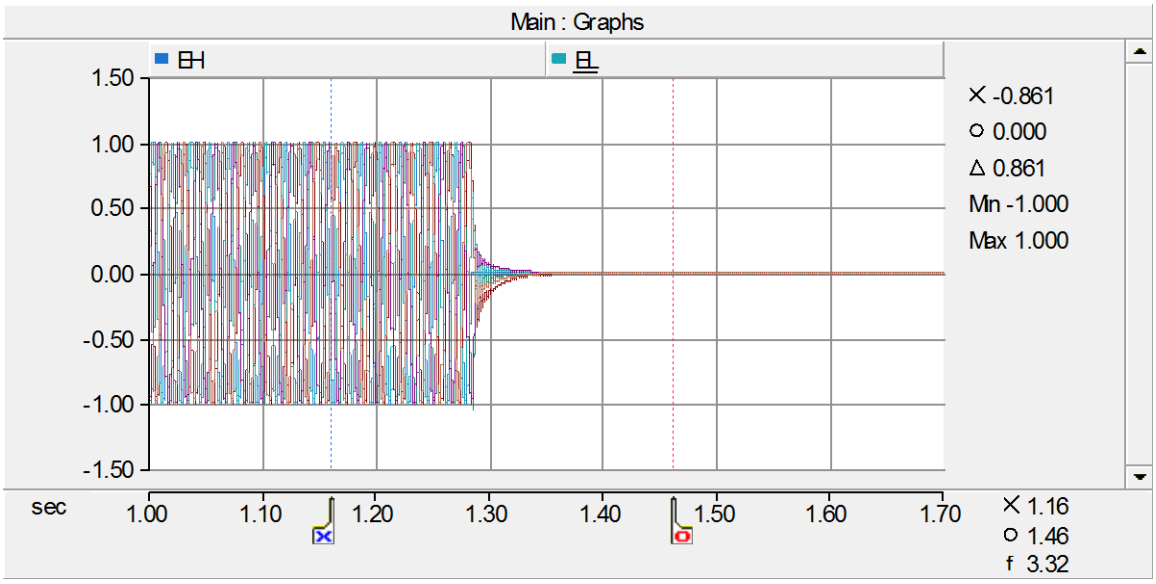


Delta Side Voltage with INVERTER#3_1 MW

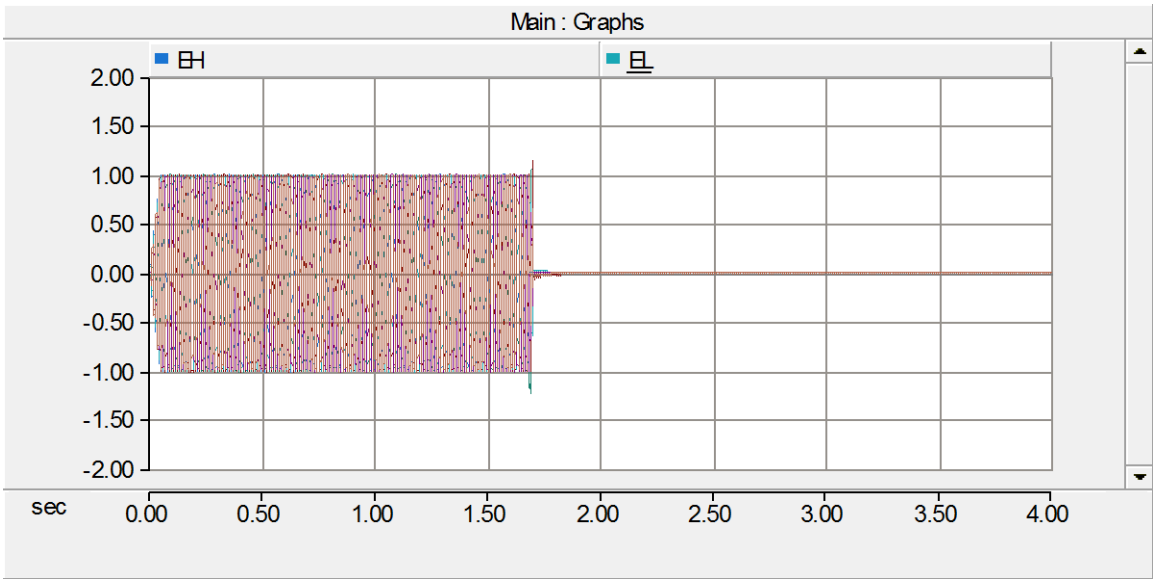
4.2.2. Scenario#2



Delta Side Voltage with INVERTER#1_250 KW

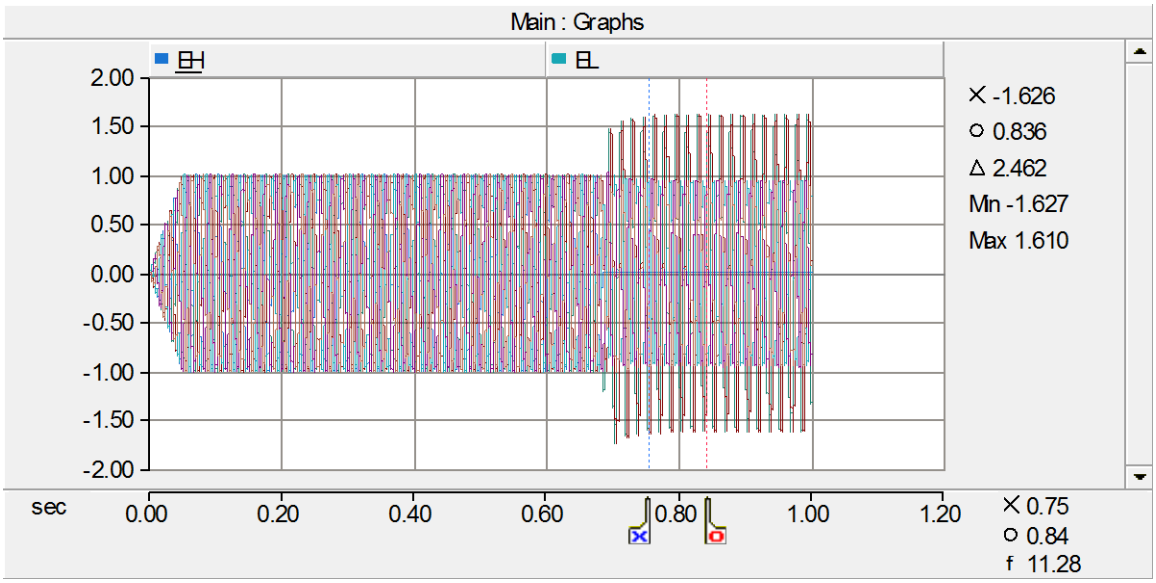


Delta Side Voltage with Inverter#2_250 KW

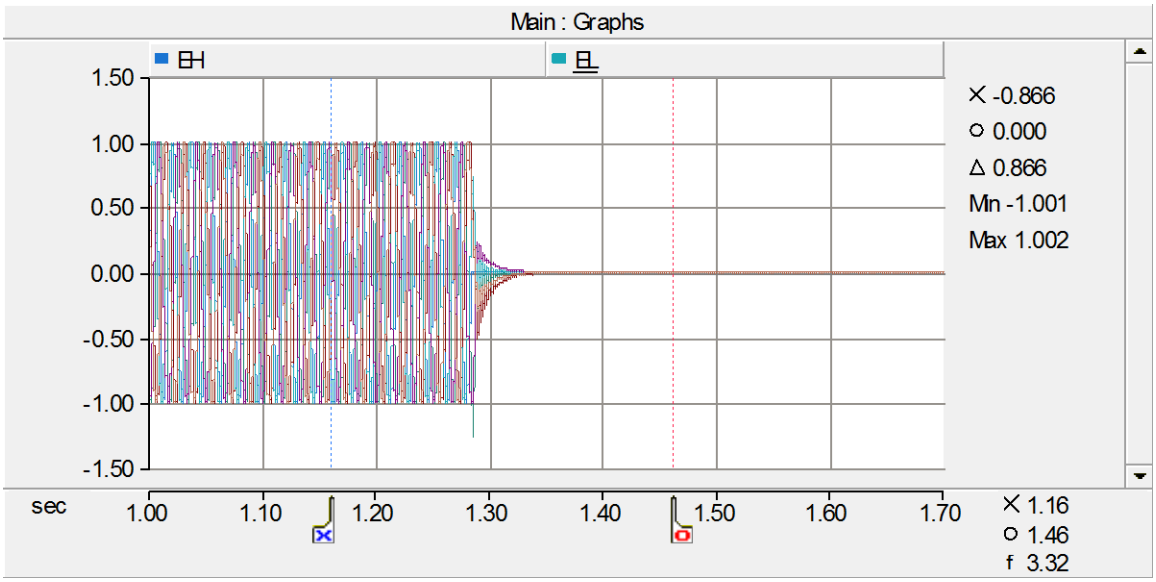


Delta Side Voltage with INVERTER#3_1 MW

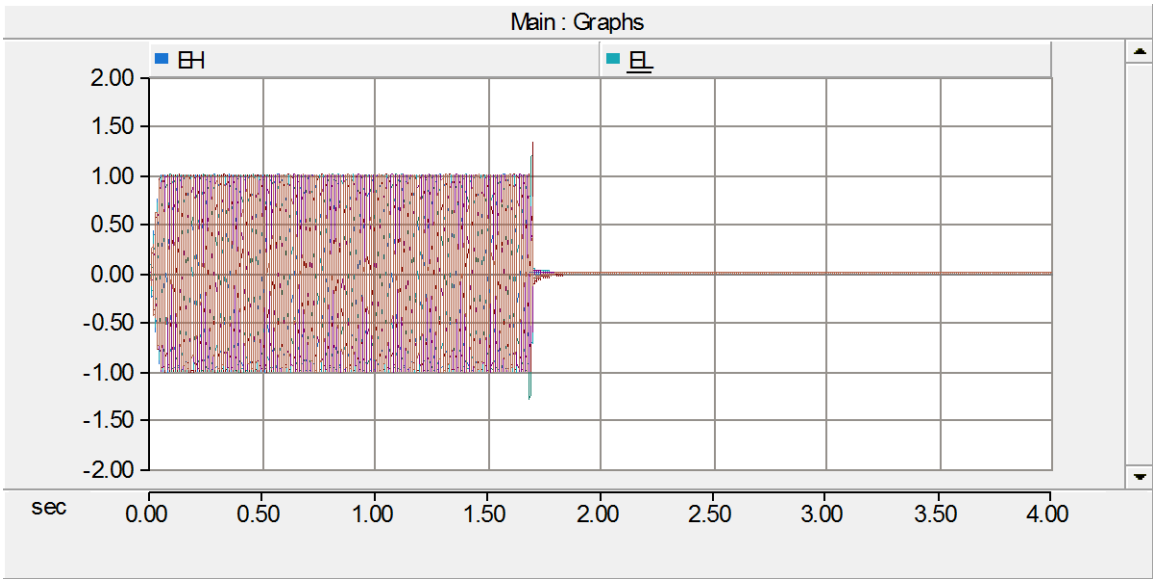
4.2.3. Scenario#3



Delta Side Voltage with INVERTER#1_250 KW

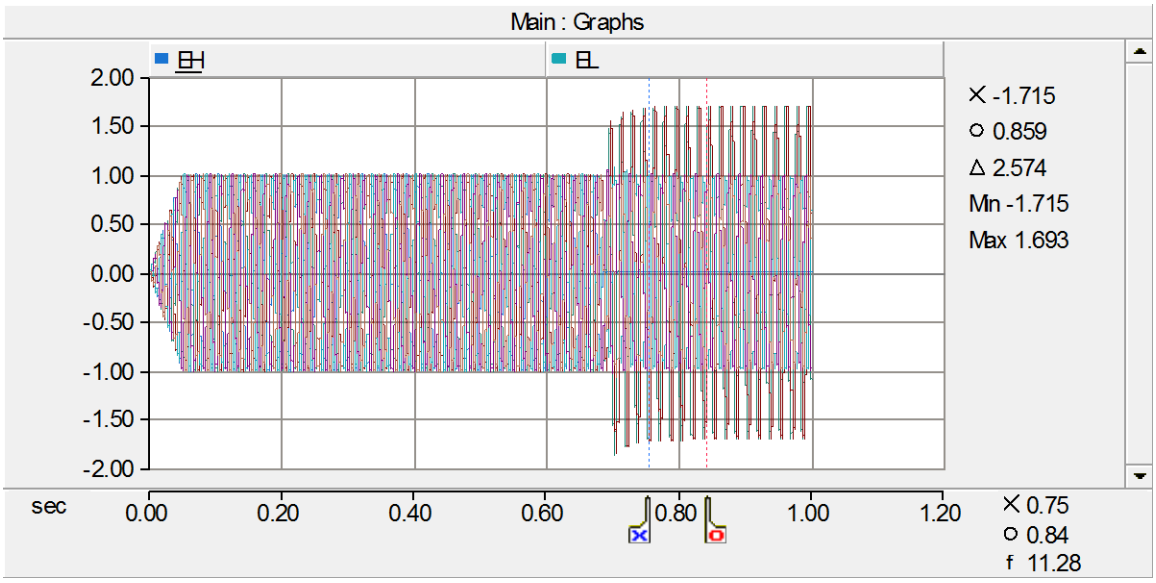


Delta Side Voltage with Inverter#2_250 KW

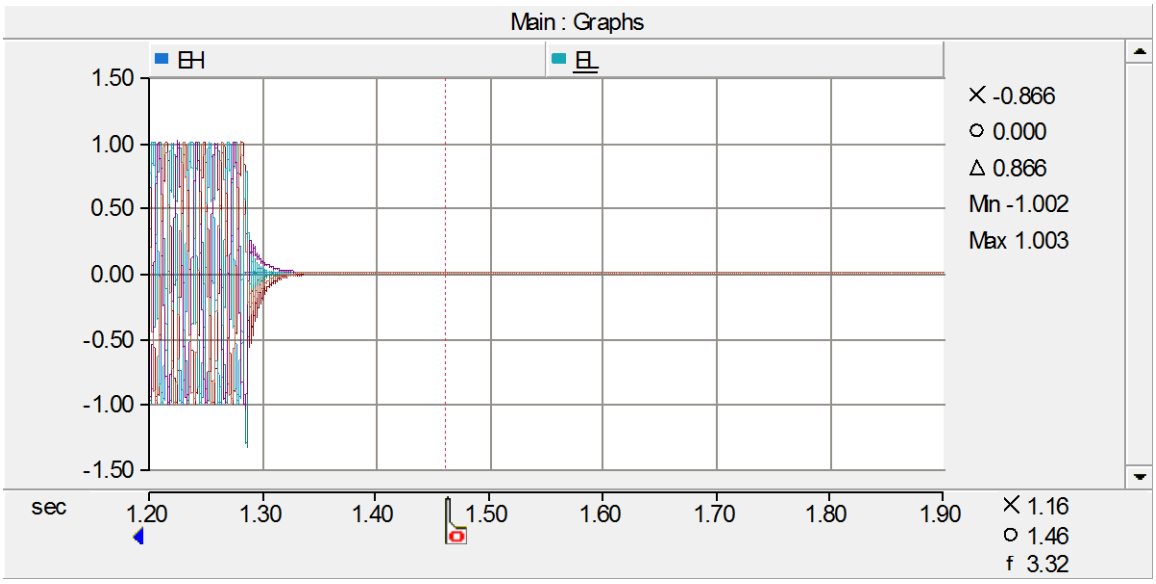


Delta Side Voltage with INVERTER#3_1 MW

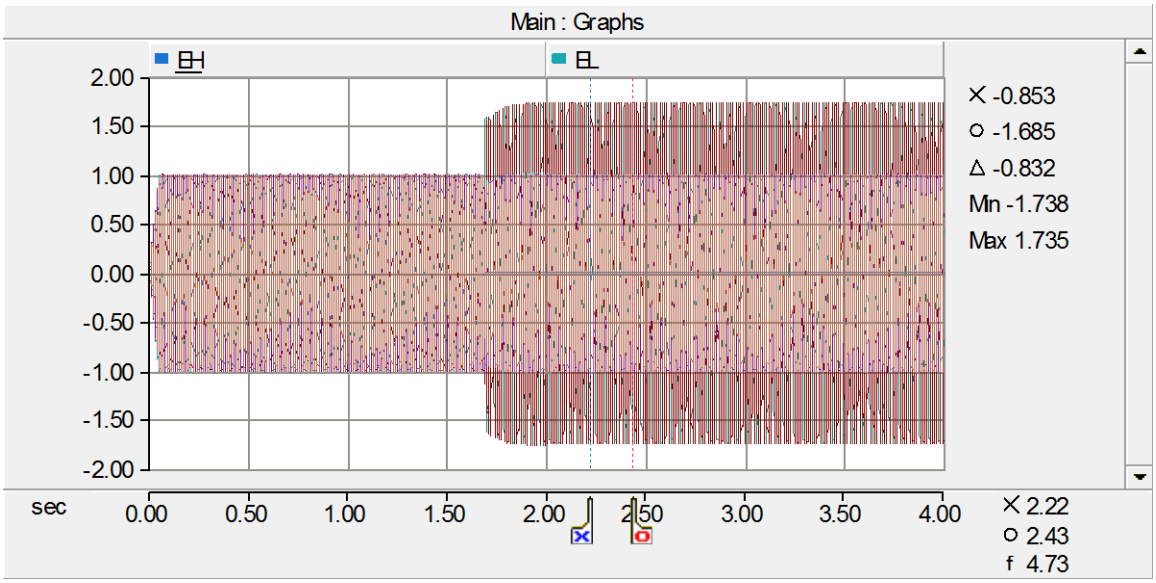
4.2.4. Scenario#4



Delta Side Voltage with INVERTER#1_250 KW

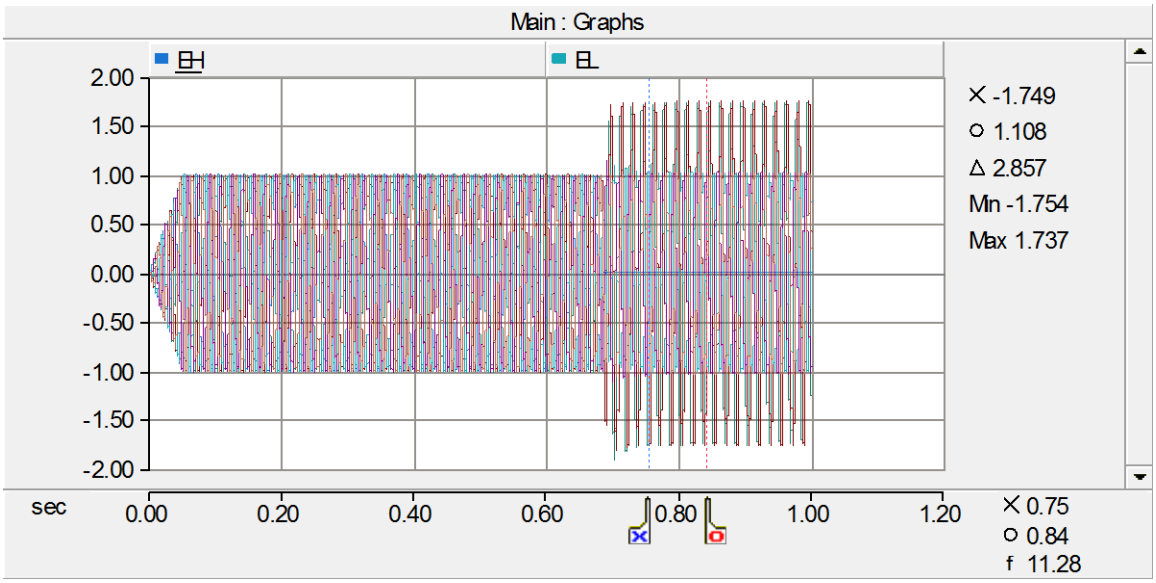


Delta Side Voltage with Inverter#2_250 KW

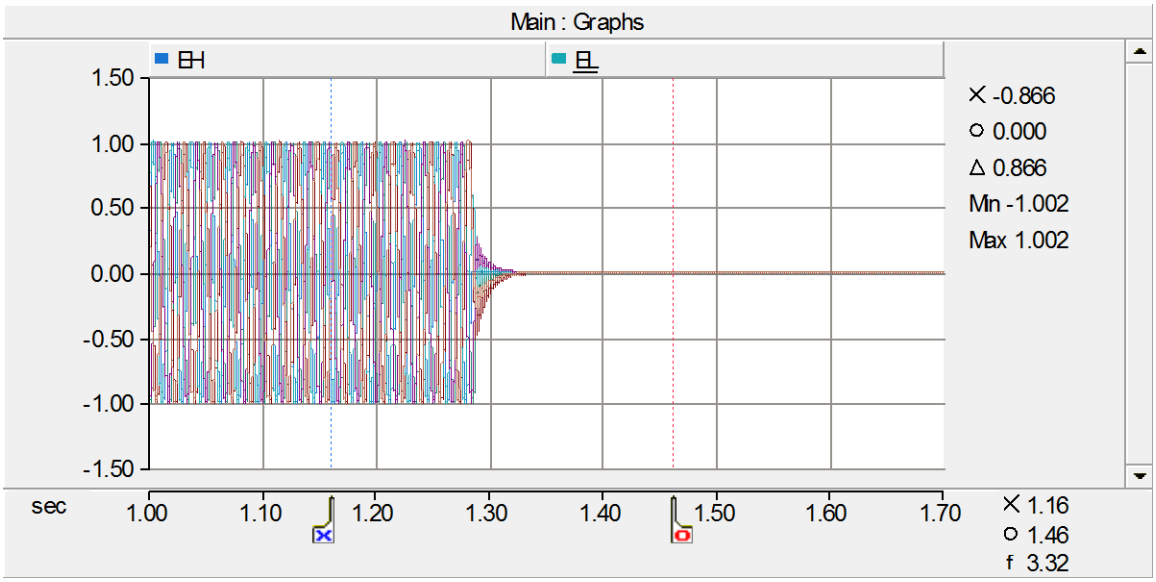


Delta Side Voltage with INVERTER#3_1 MW

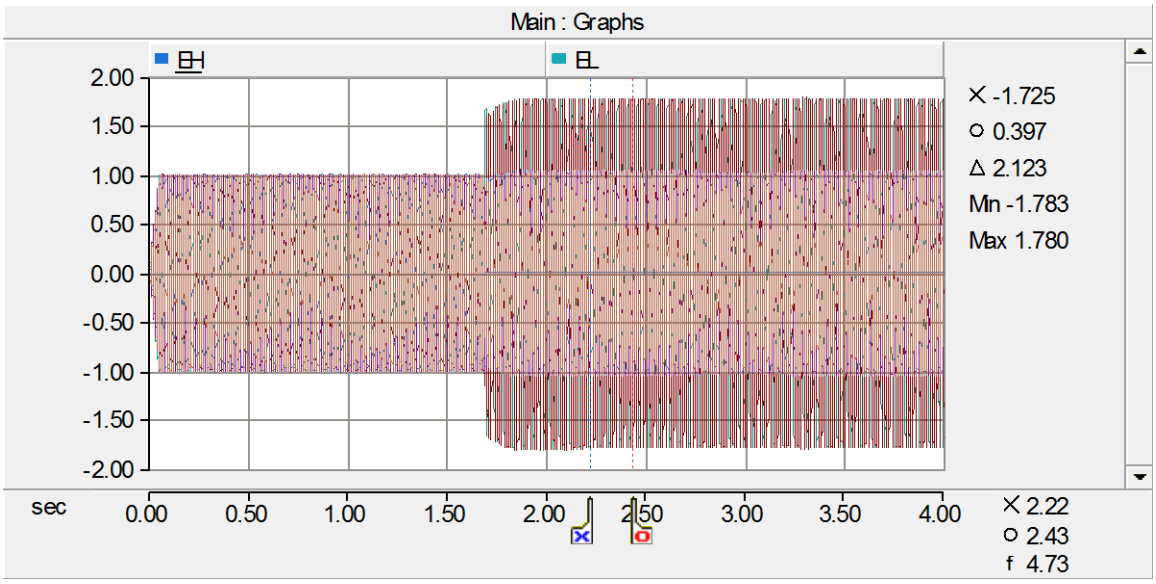
4.2.5. Scenario#5



Delta Side Voltage with INVERTER#1_250 KW

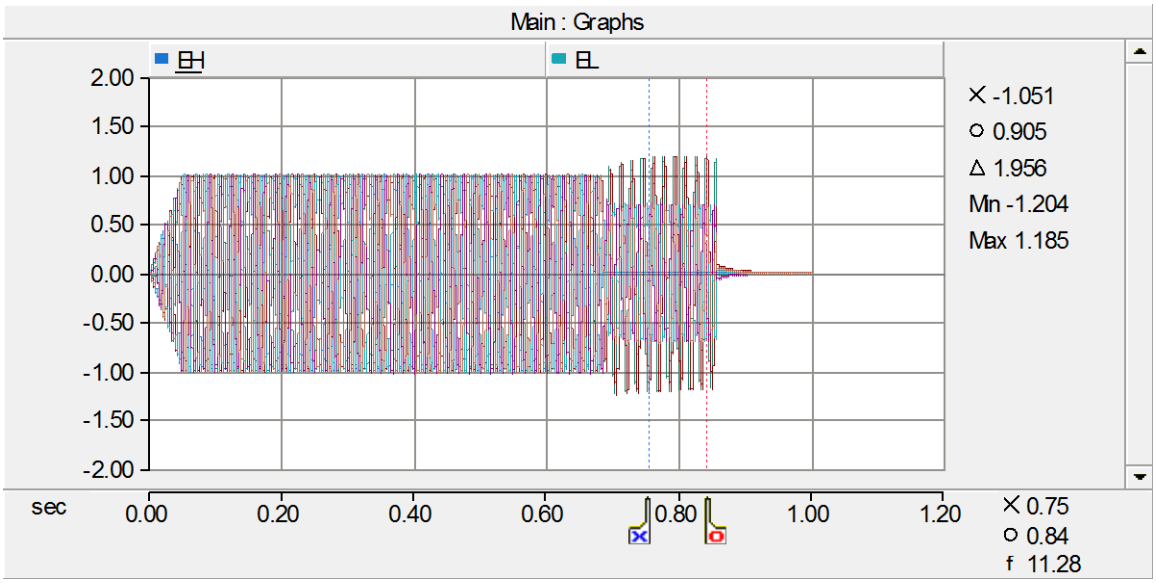


Delta Side Voltage with Inverter#2_250 KW

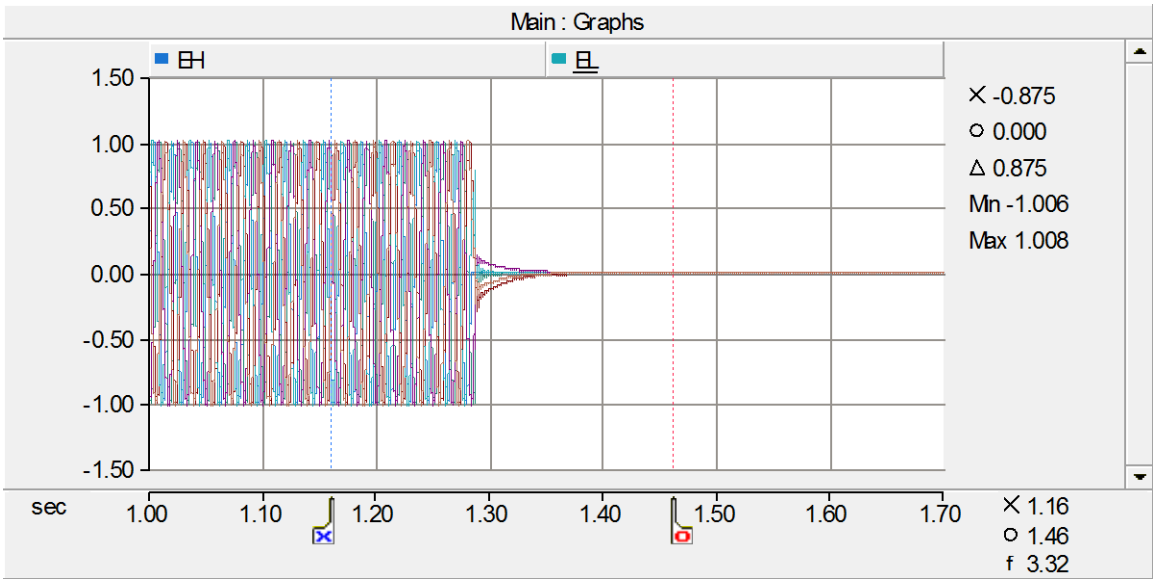


Delta Side Voltage with INVERTER#3_1 MW

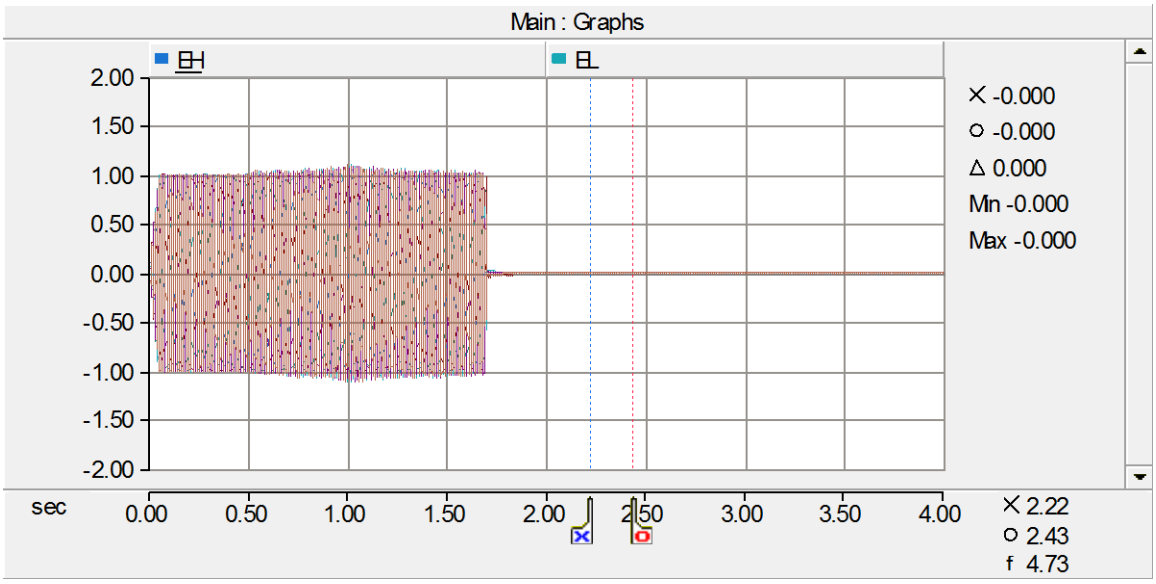
4.2.6. Scenario#6



Delta Side Voltage with INVERTER#1_250 KW

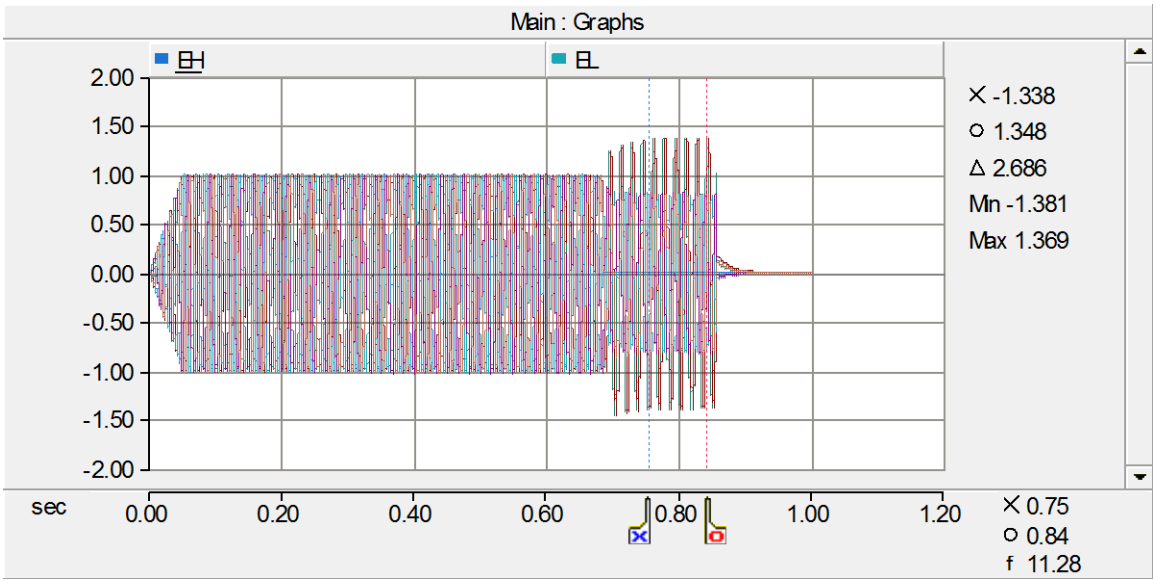


Delta Side Voltage with Inverter#2_250 KW

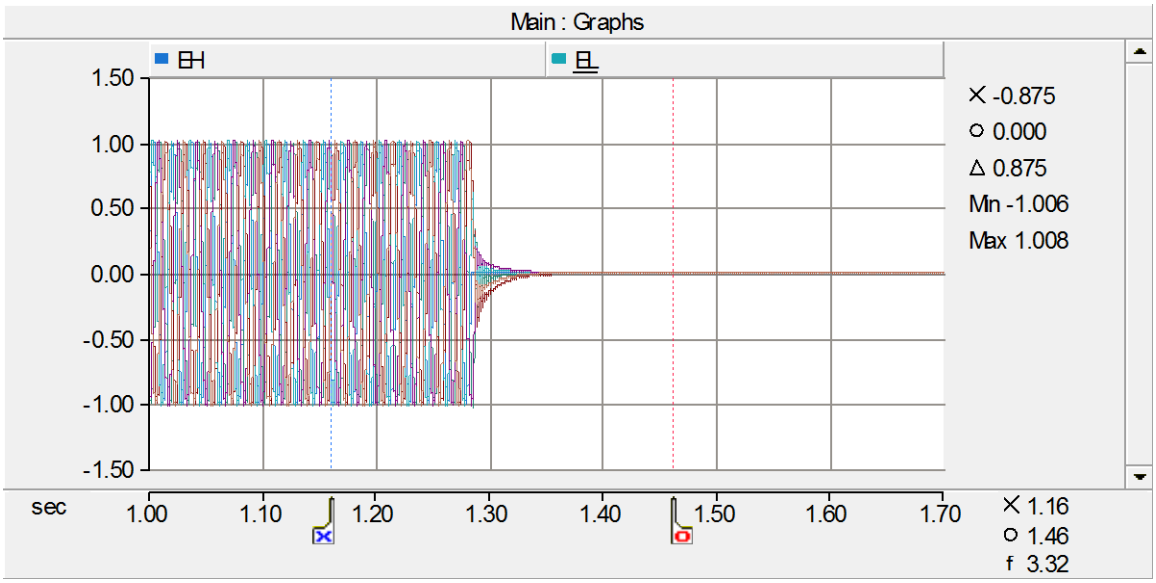


Delta Side Voltage with INVERTER#3_1 MW

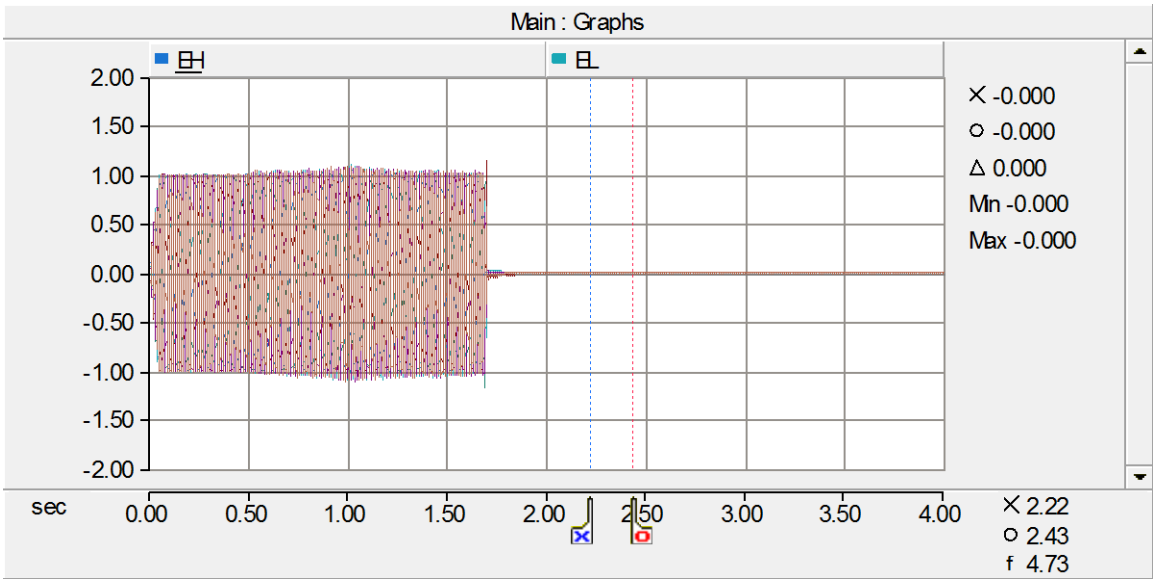
4.2.7. Scenario#7



Delta Side Voltage with INVERTER#1_250 KW

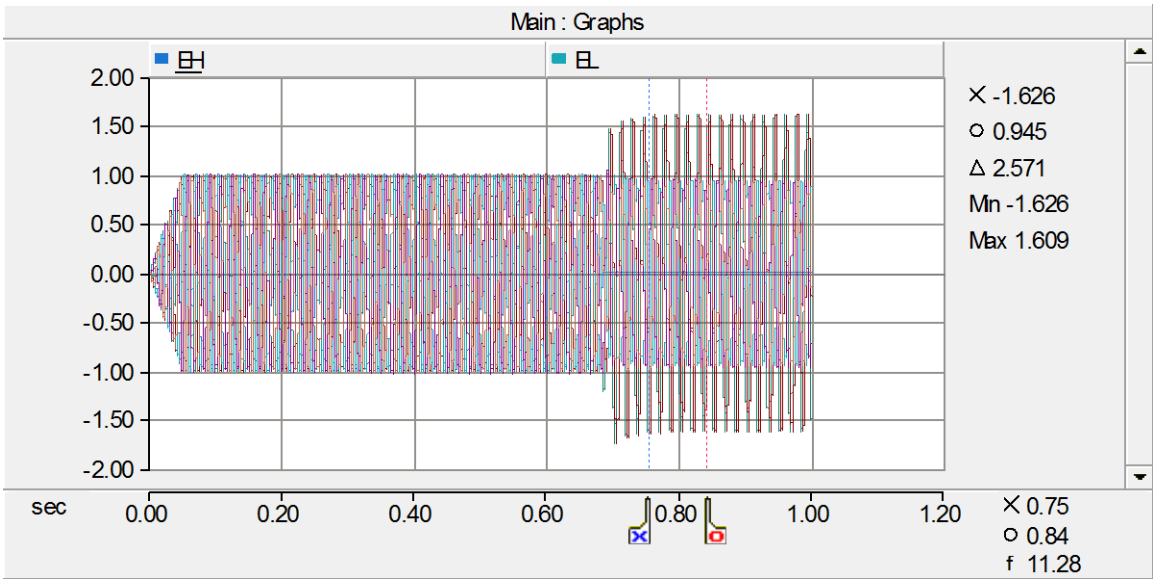


Delta Side Voltage with Inverter#2_250 KW

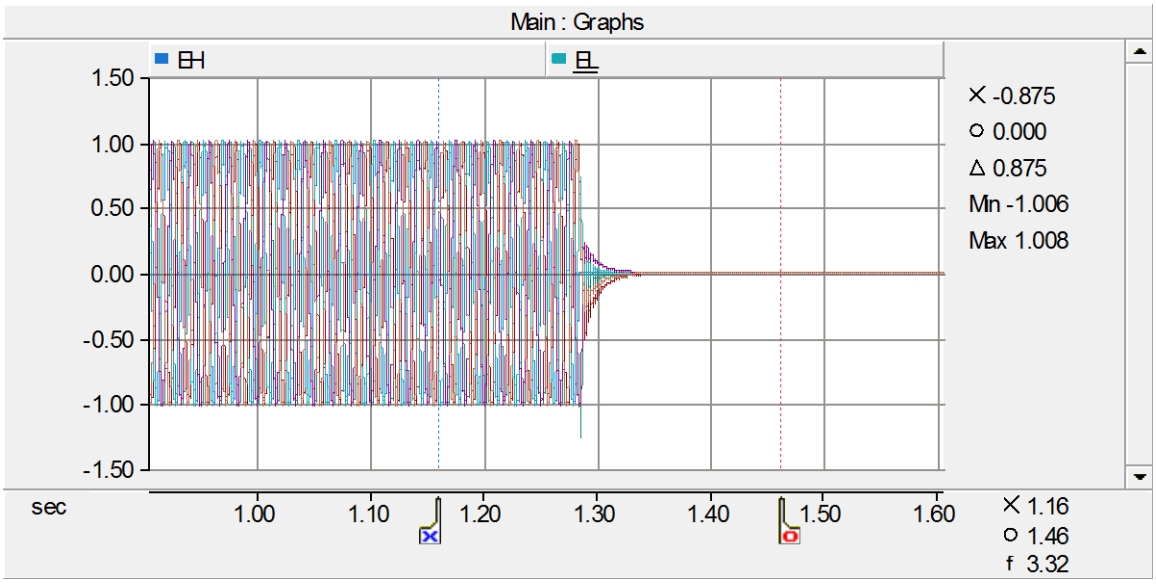


Delta Side Voltage with INVERTER#3_1 MW

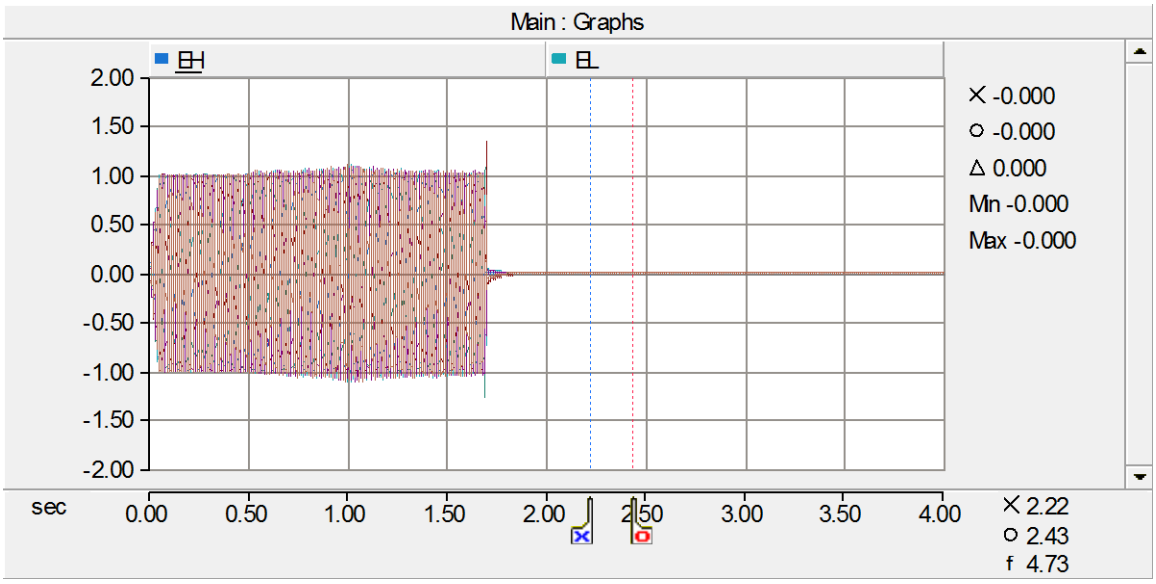
4.2.8. Scenario#8



Delta Side Voltage with INVERTER#1_250 KW

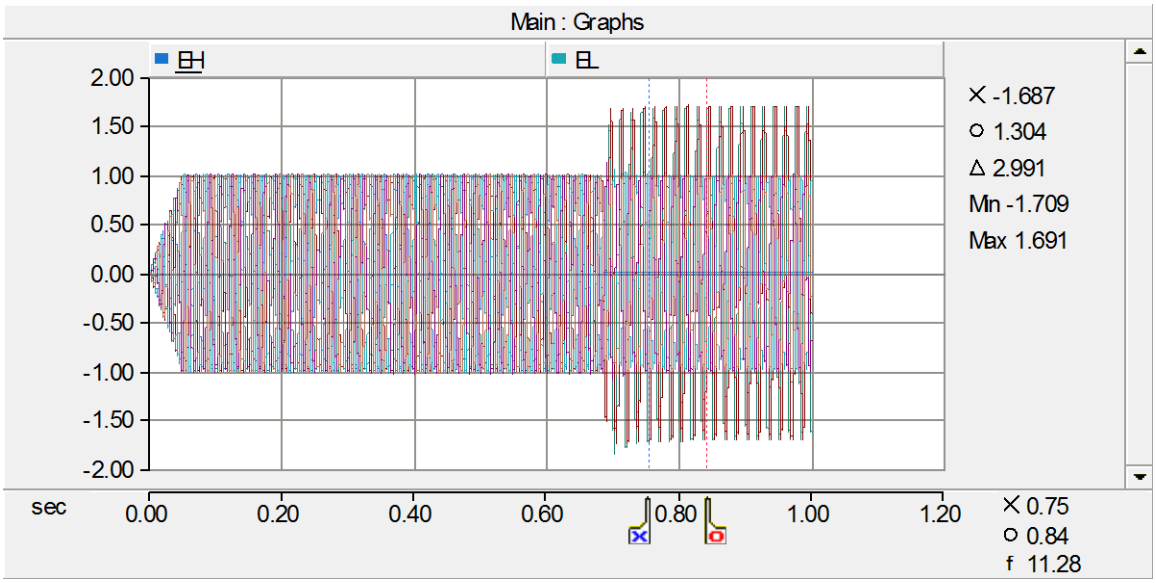


Delta Side Voltage with Inverter#2_250 KW

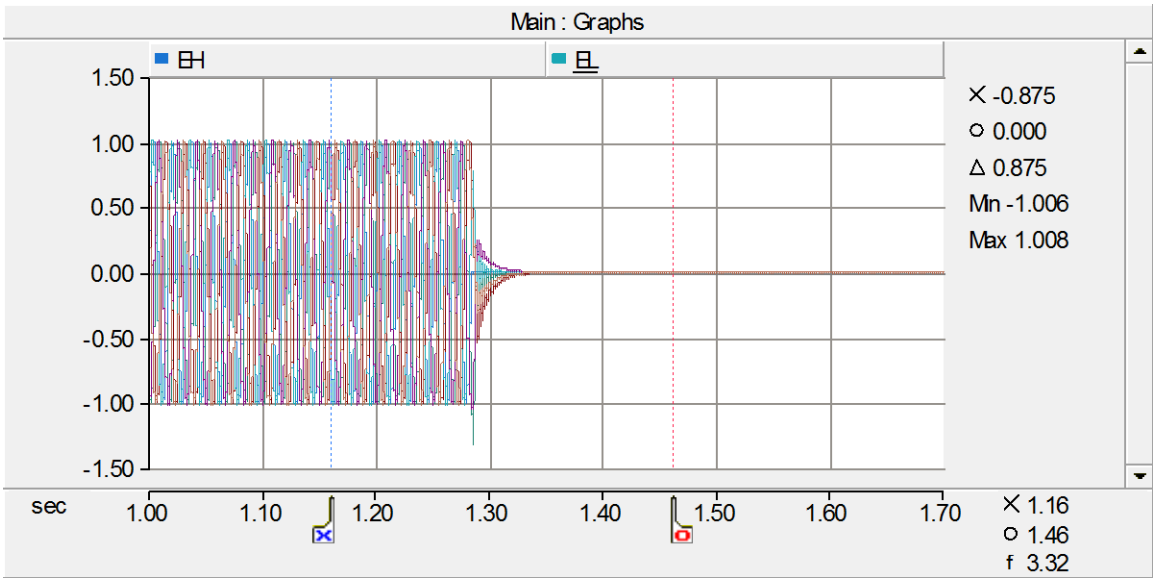


Delta Side Voltage with INVERTER#3_1 MW

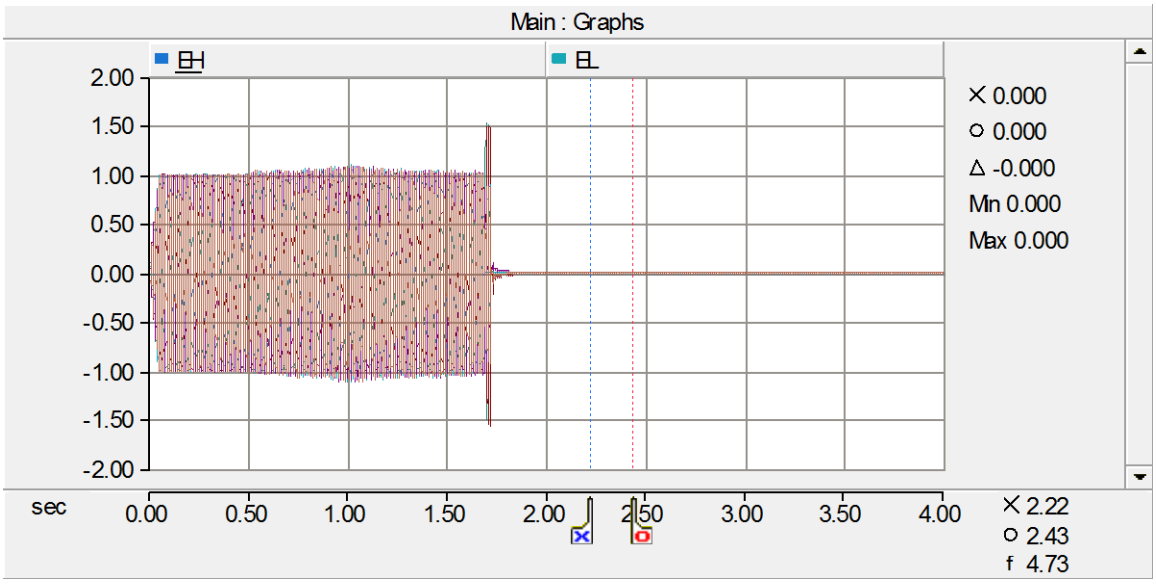
4.2.9. Scenario#9



Delta Side Voltage with INVERTER#1_250 KW

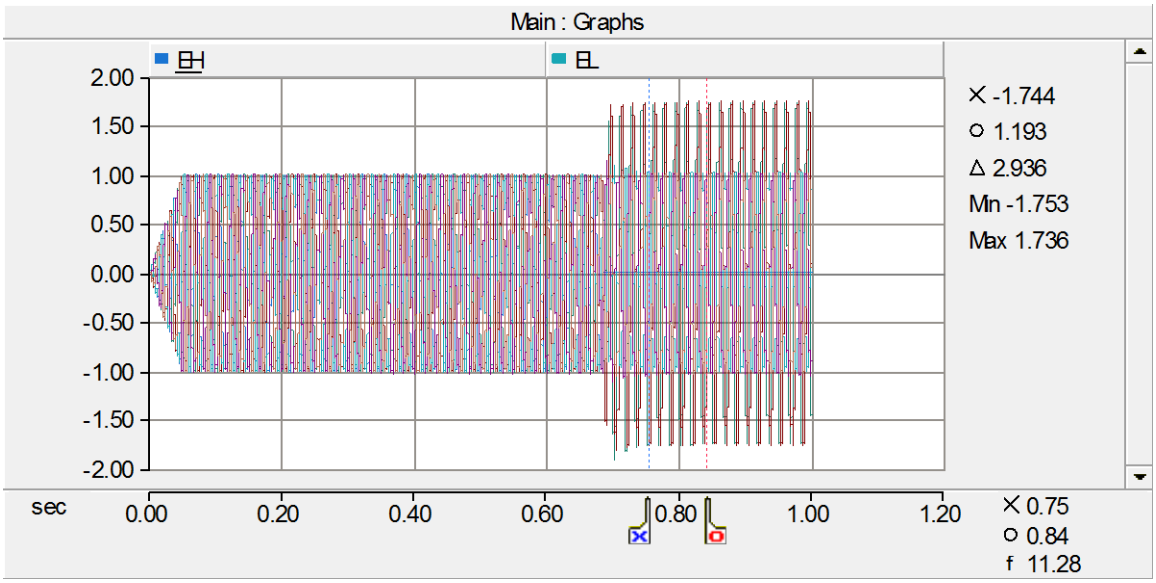


Delta Side Voltage with Inverter#2_250 KW

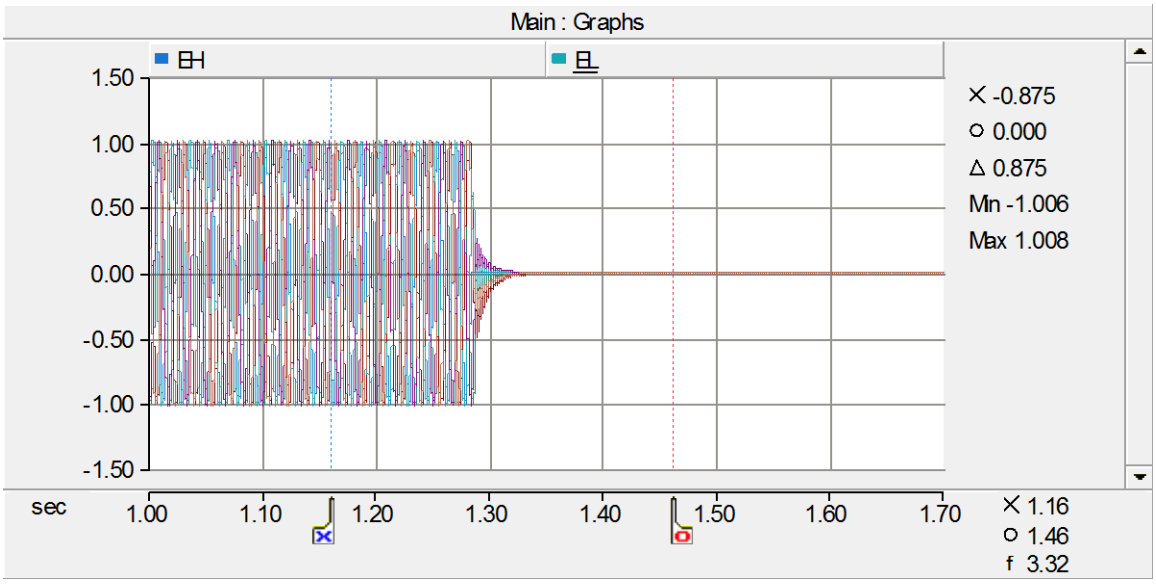


Delta Side Voltage with INVERTER#3_1 MW

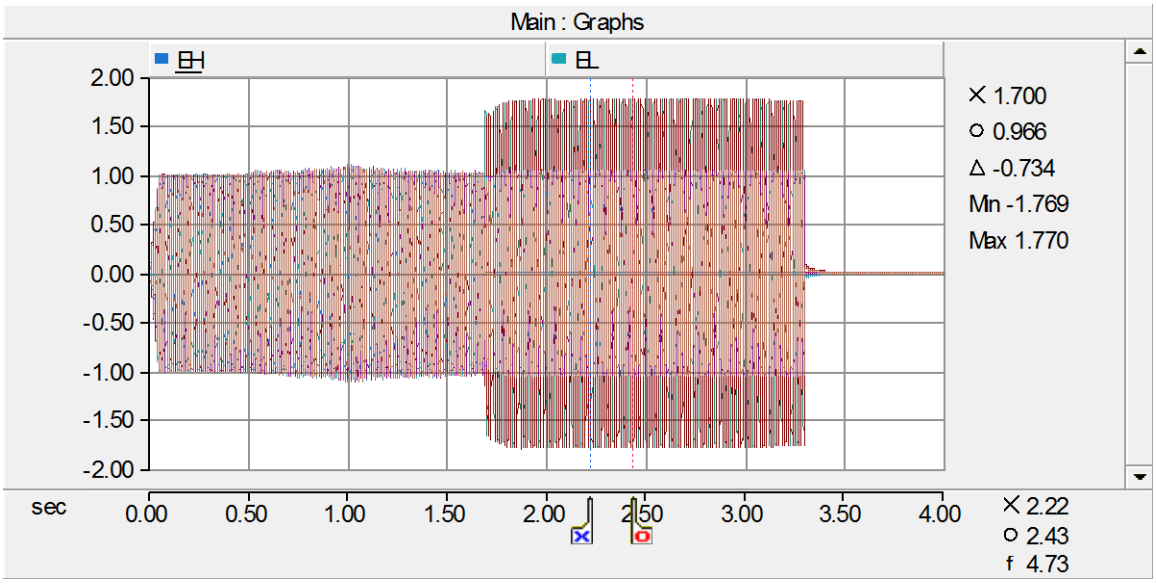
4.2.10. Scenario#10



Delta Side Voltage with INVERTER#1_250 KW

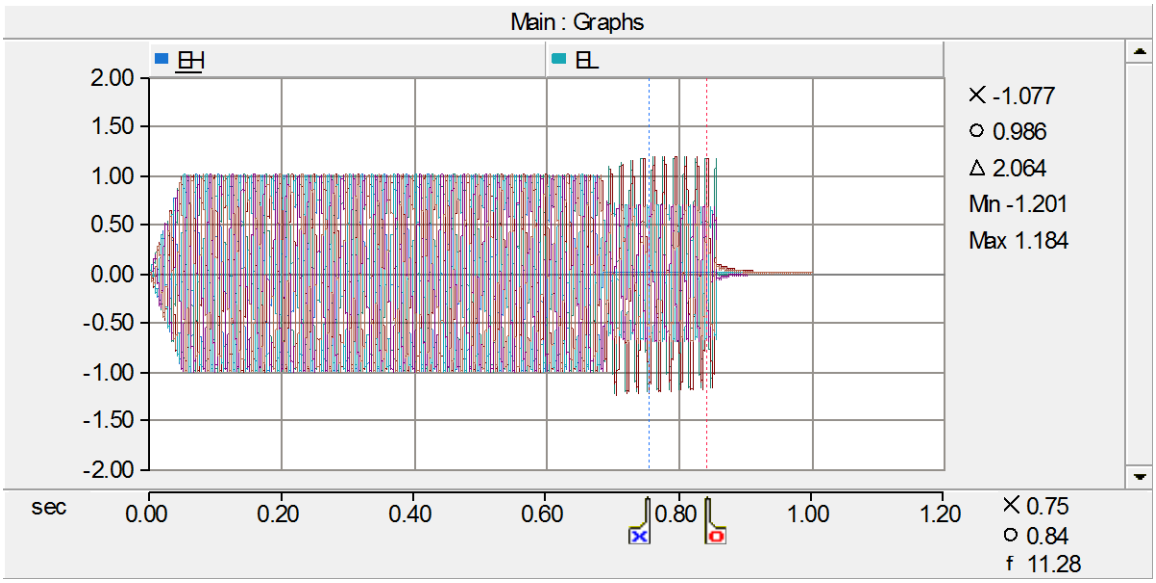


Delta Side Voltage with Inverter#2_250 KW

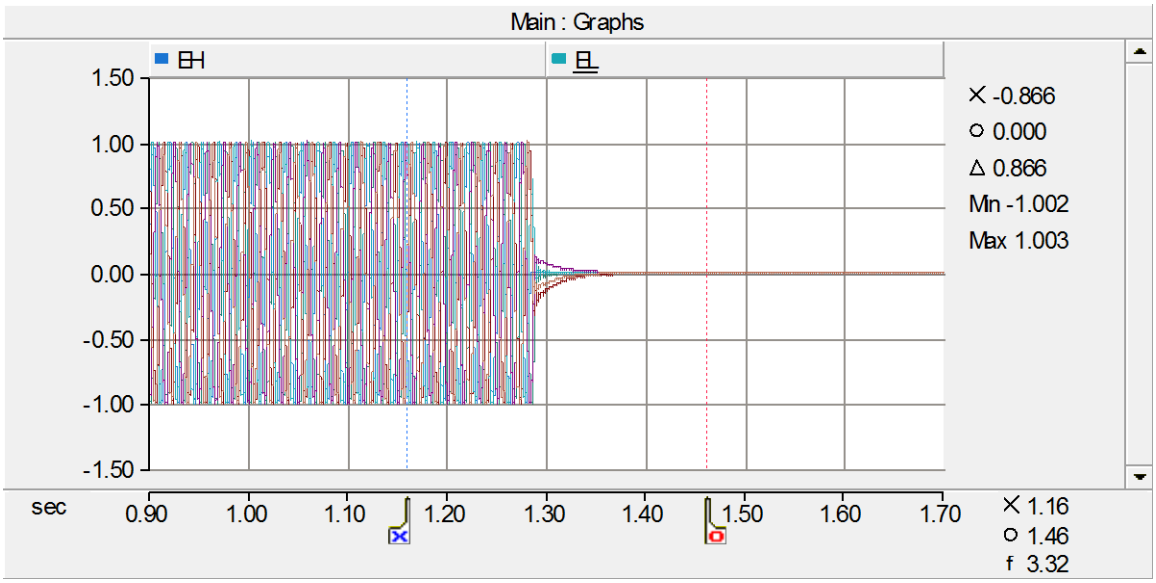


Delta Side Voltage with INVERTER#3_1 MW

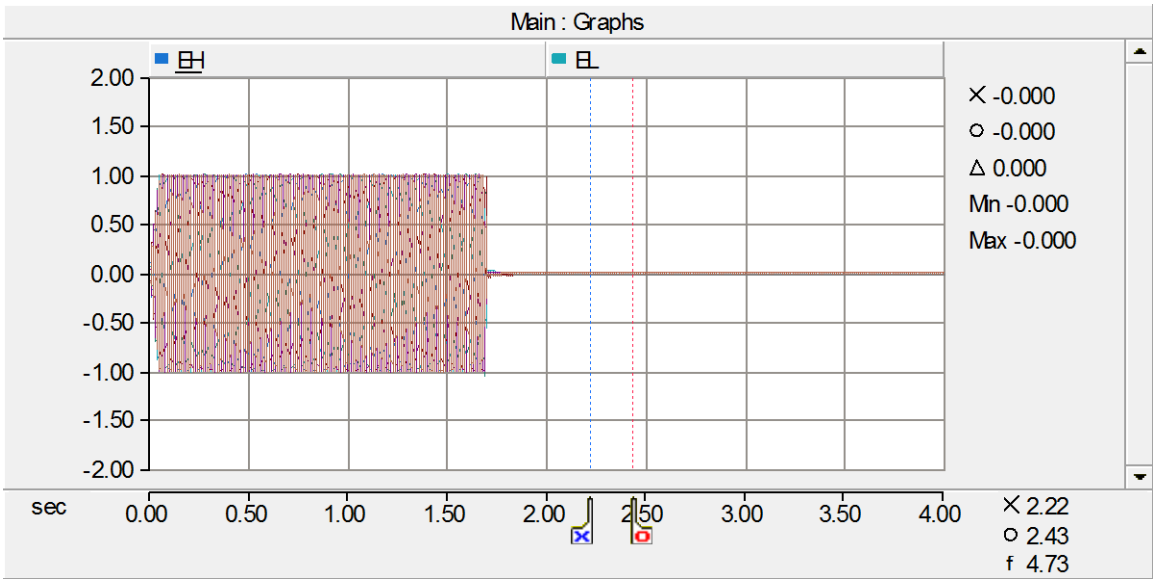
4.2.11. Scenario#11



Delta Side Voltage with INVERTER#1_250 KW

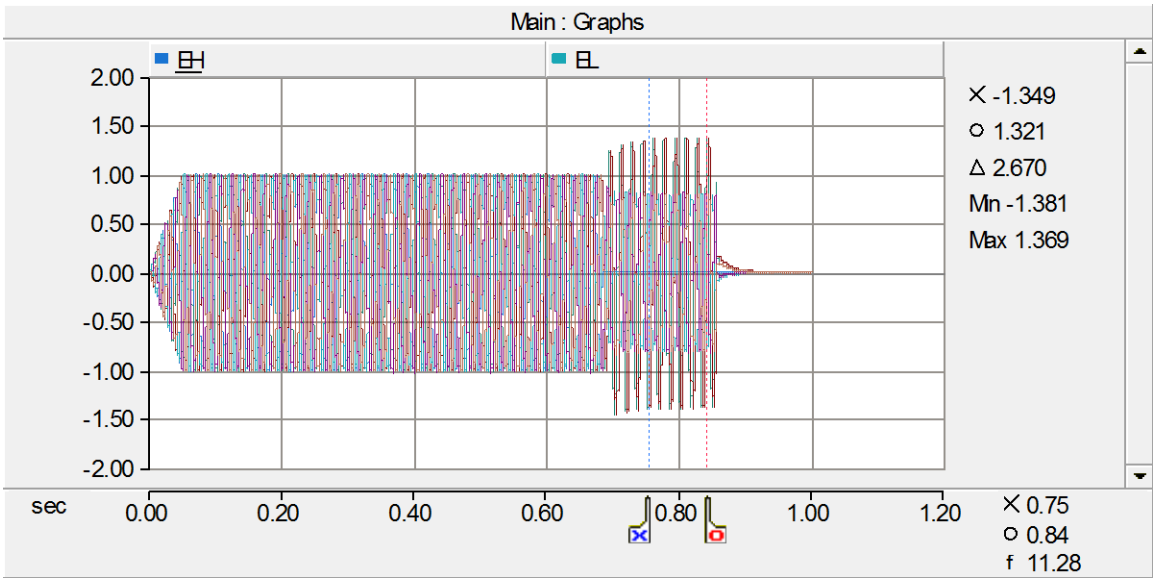


Delta Side Voltage with Inverter#2_250 KW

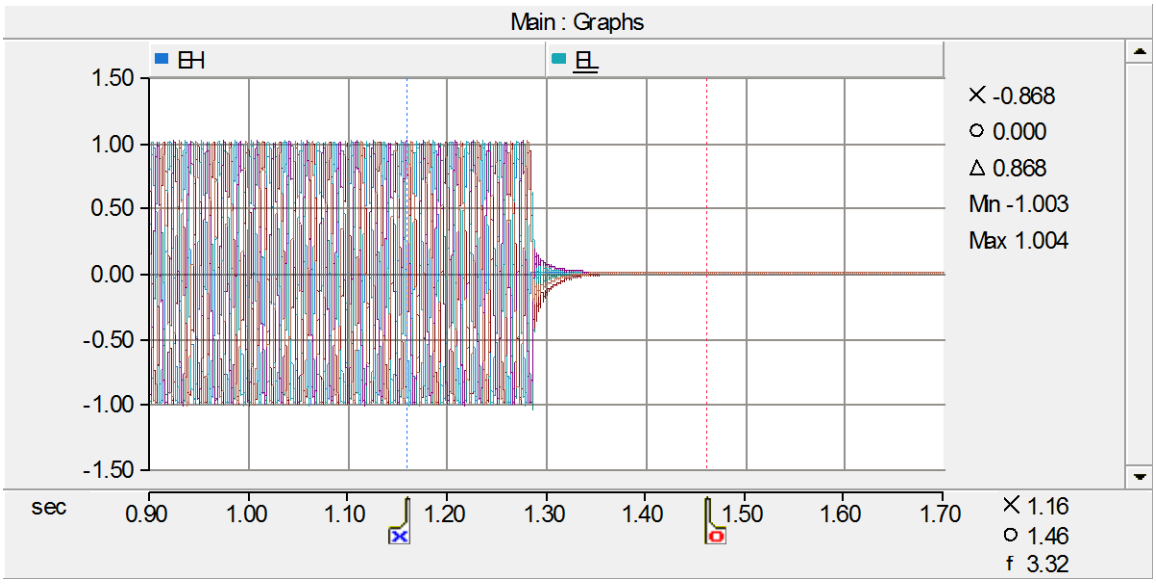


Delta Side Voltage with INVERTER#3_1 MW

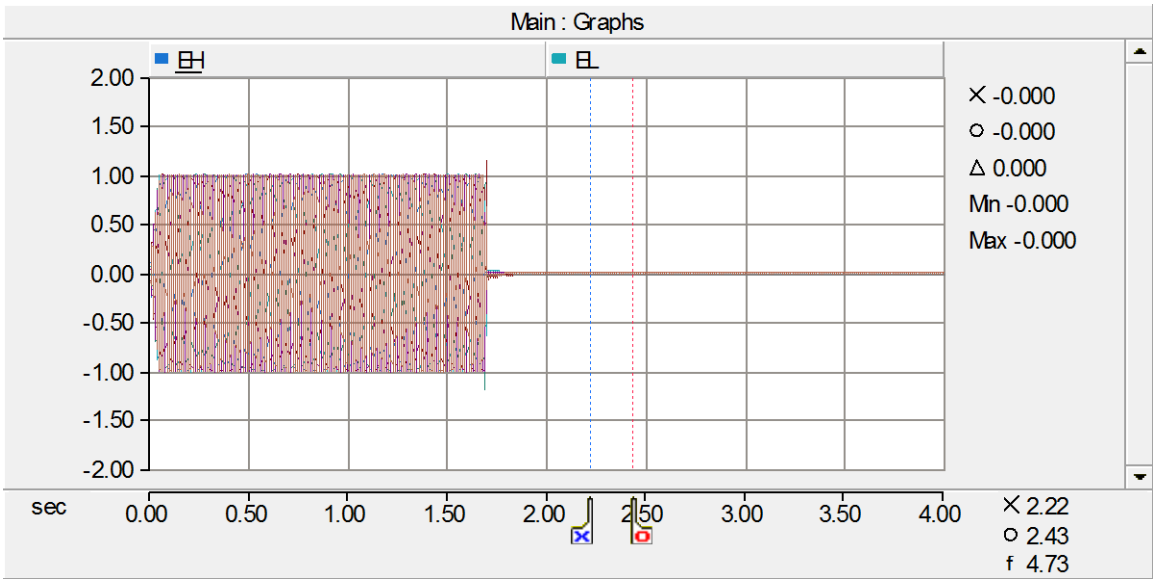
4.2.12. Scenario#12



Delta Side Voltage with INVERTER#1_250 KW

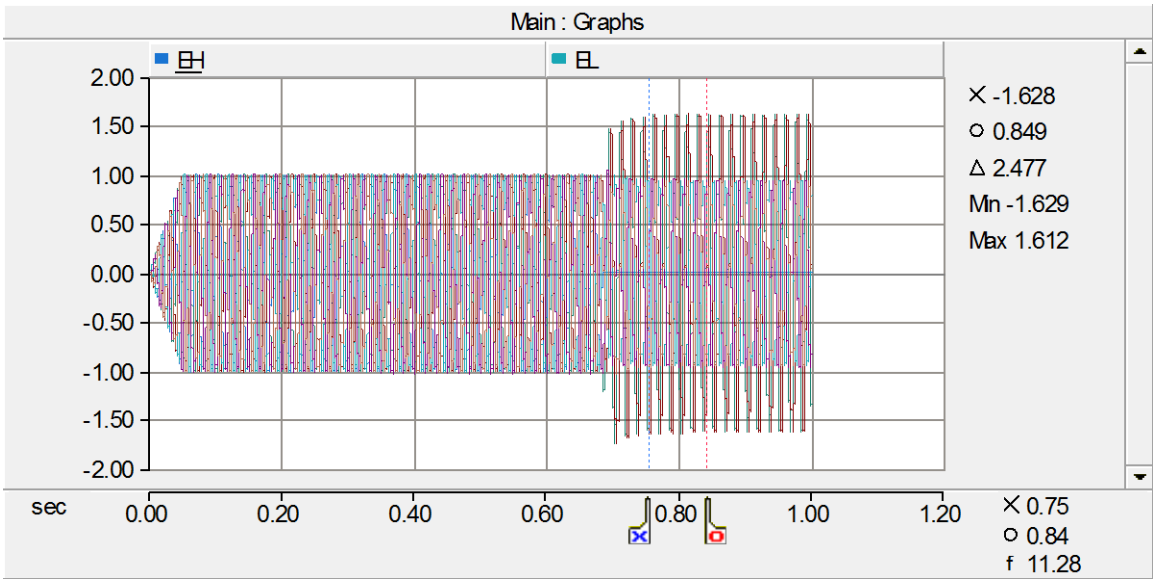


Delta Side Voltage with Inverter#2_250 KW

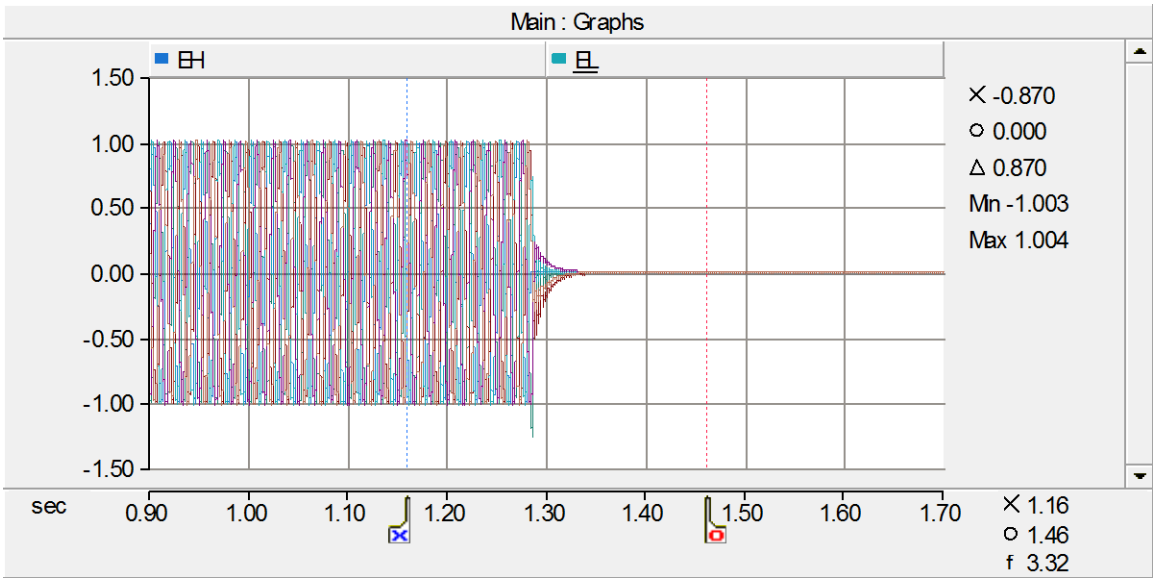


Delta Side Voltage with INVERTER#3_1 MW

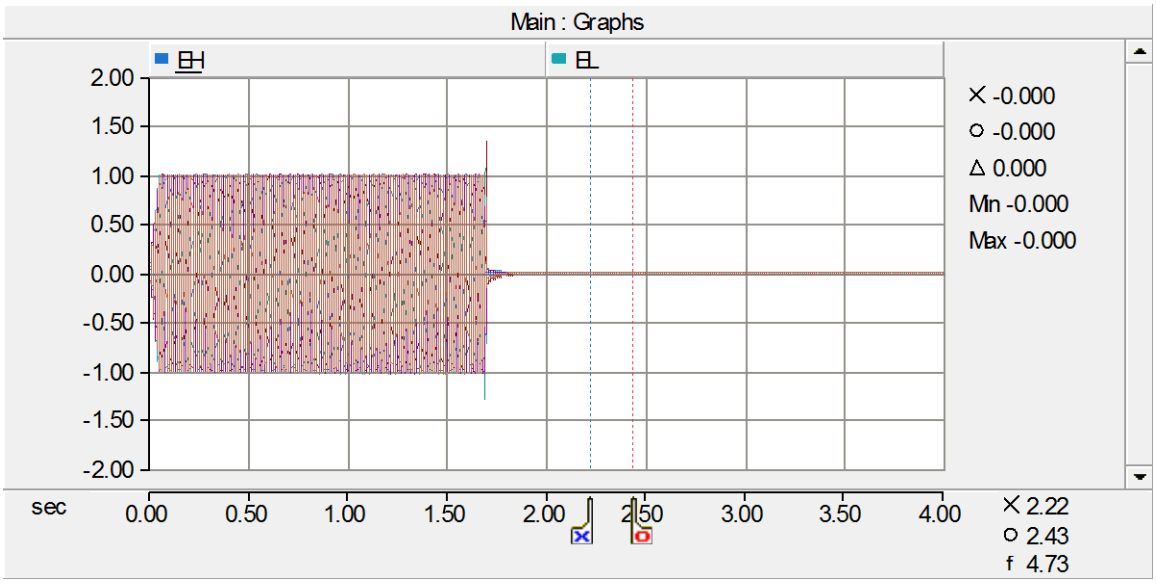
4.2.13. Scenario#13



Delta Side Voltage with INVERTER#1_250 KW

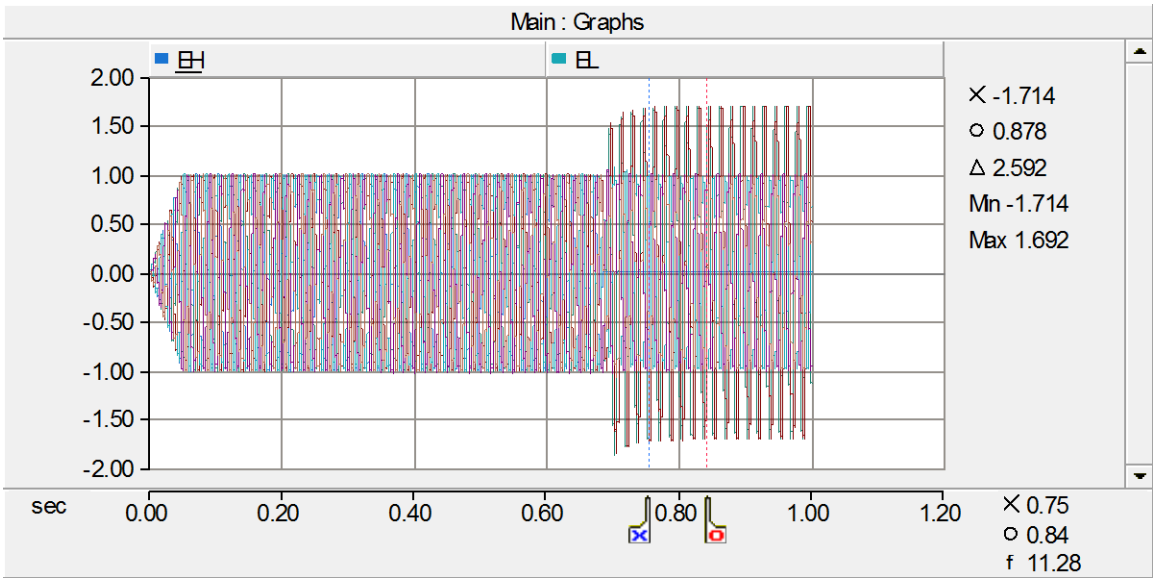


Delta Side Voltage with Inverter#2_250 KW

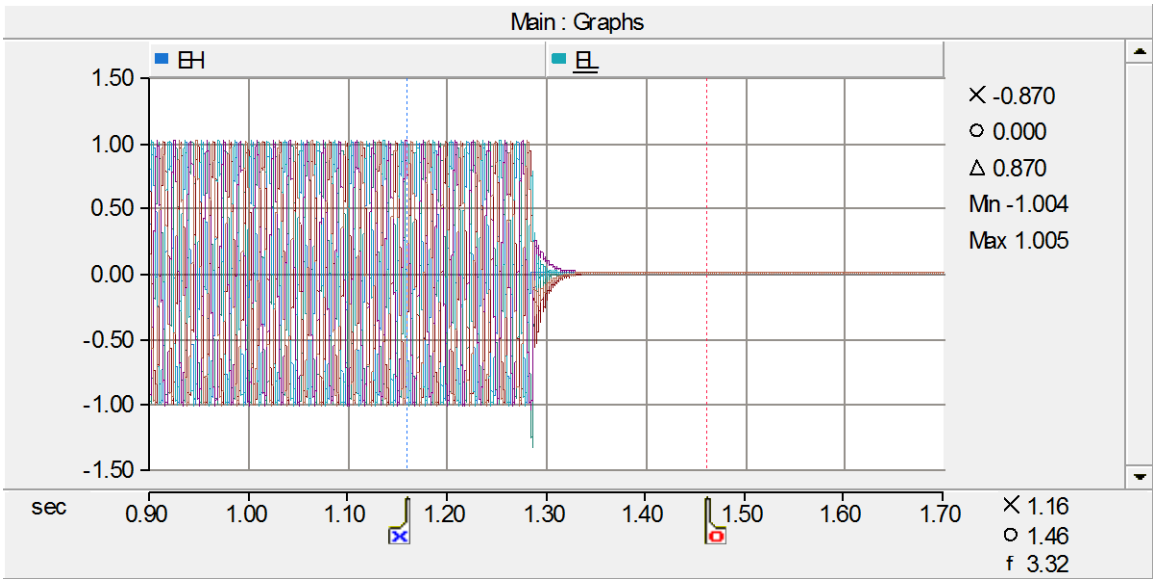


Delta Side Voltage with INVERTER#3_1 MW

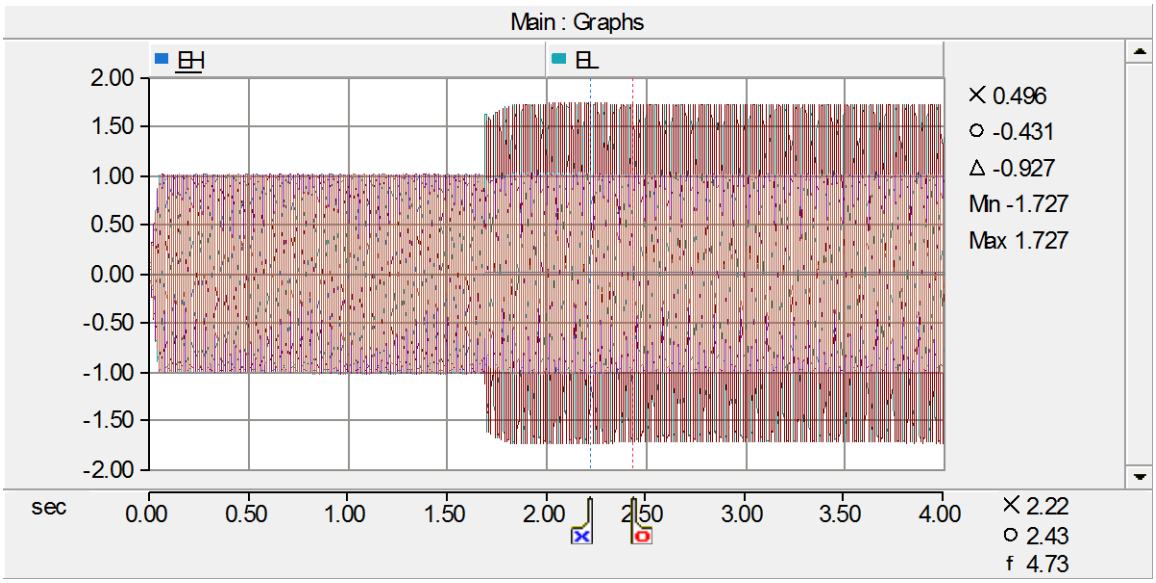
4.2.14. Scenario#14



Delta Side Voltage with INVERTER#1_250 KW

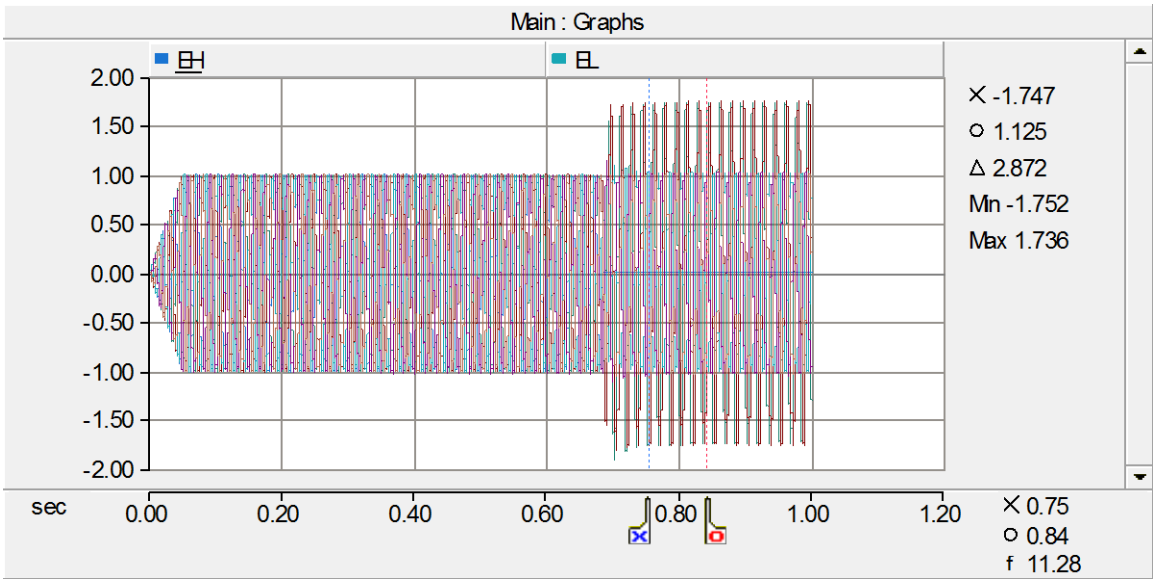


Delta Side Voltage with Inverter#2_250 KW

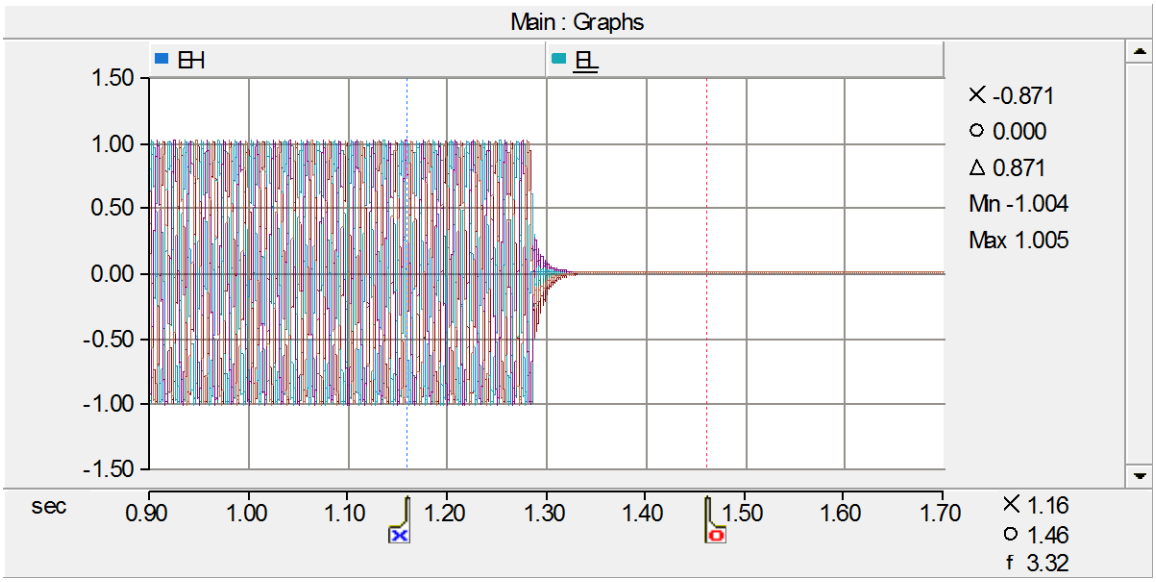


Delta Side Voltage with INVERTER#3_1 MW

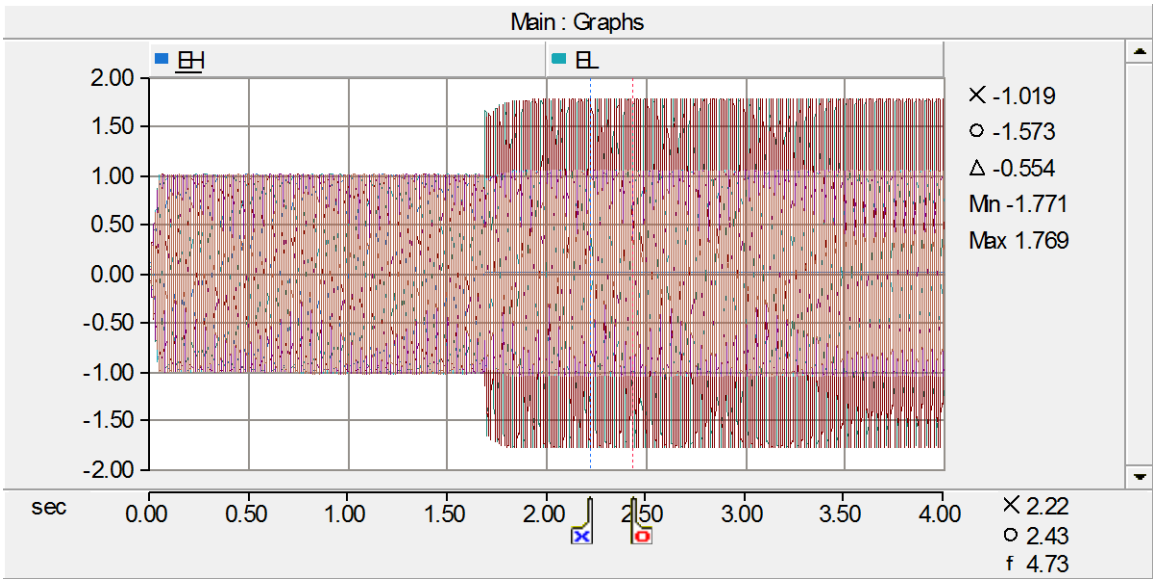
4.2.15. Scenario#15



Delta Side Voltage with INVERTER#1_250 KW

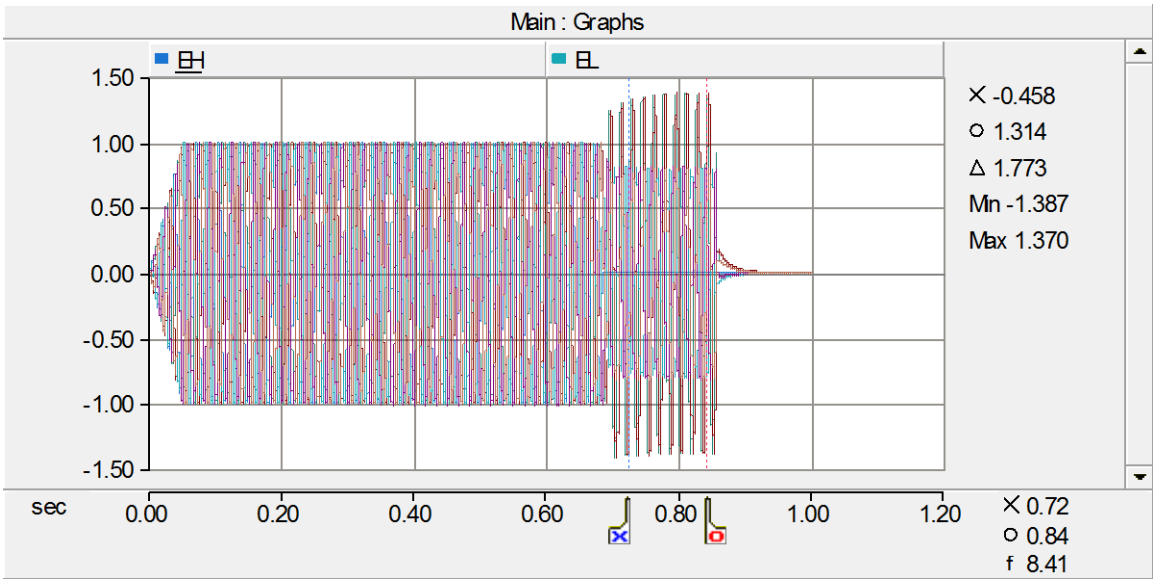


Delta Side Voltage with Inverter#2_250 KW

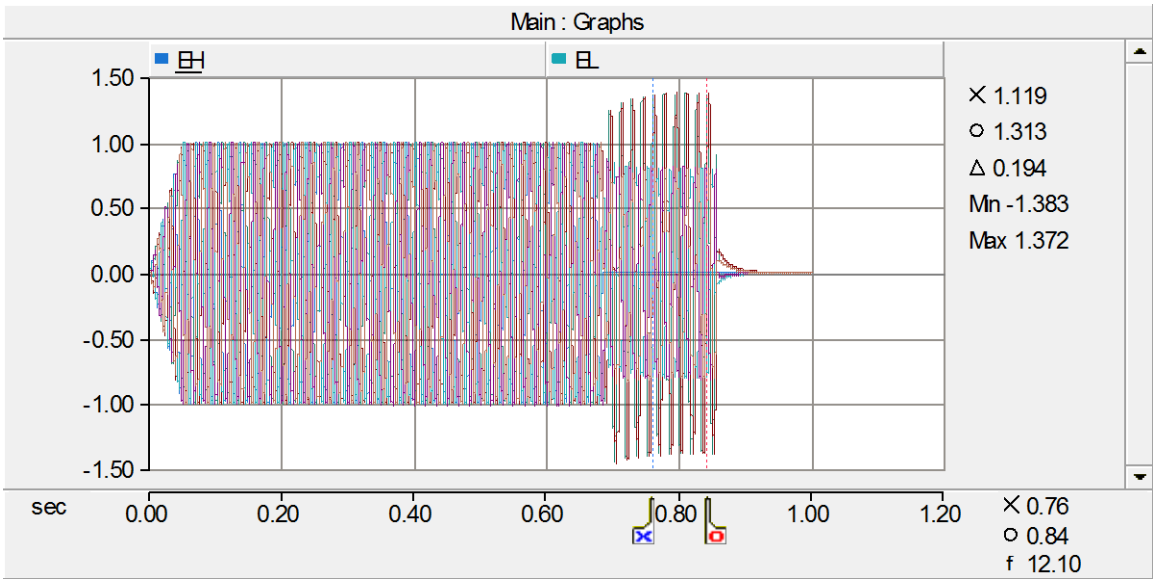


Delta Side Voltage with INVERTER#3_1 MW

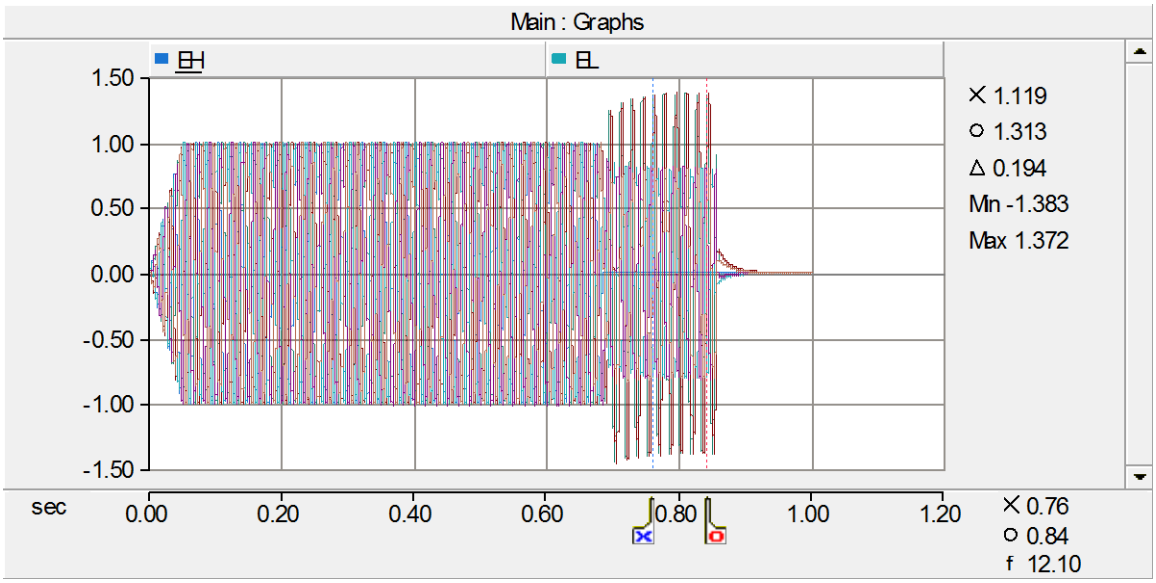
4.2.16. Scenario#16



Delta Side Voltage with Delta Side Voltage with 22KV MCOV Surge Arrester -AE 250 KW

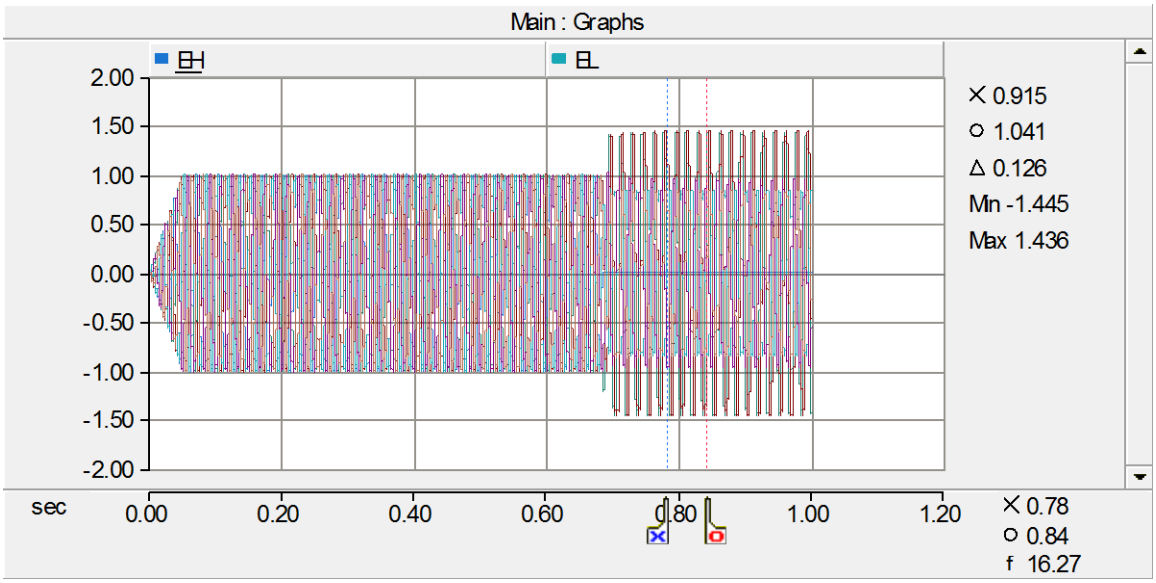


Delta Side Voltage with 24.4KV MCOV Surge Arrester -AE 250 KW

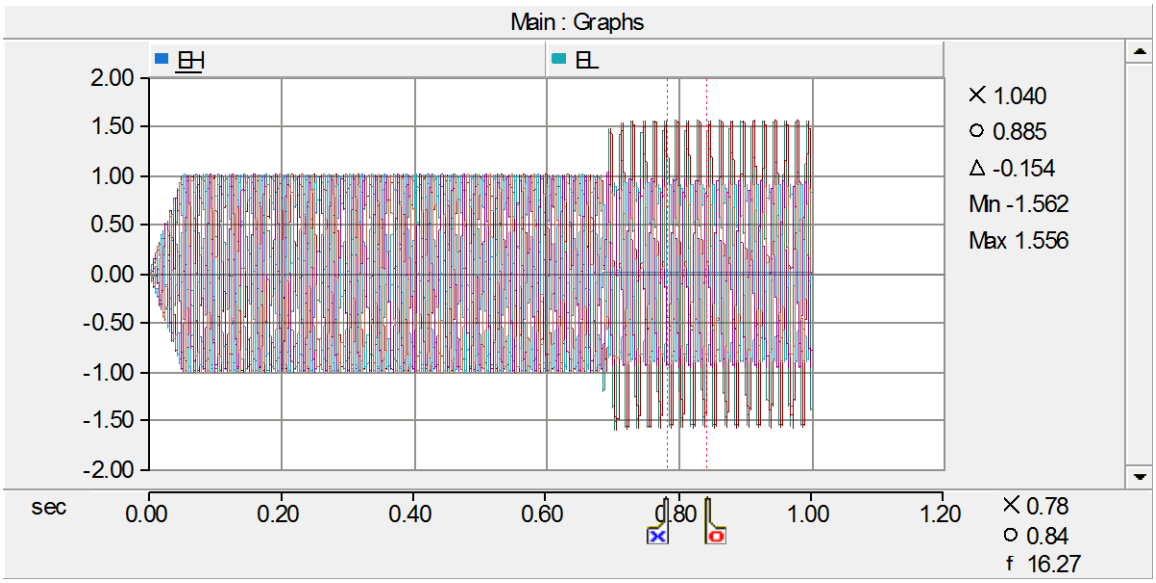


Delta Side Voltage with 29KV MCOV Surge Arrester -AE 250 KW

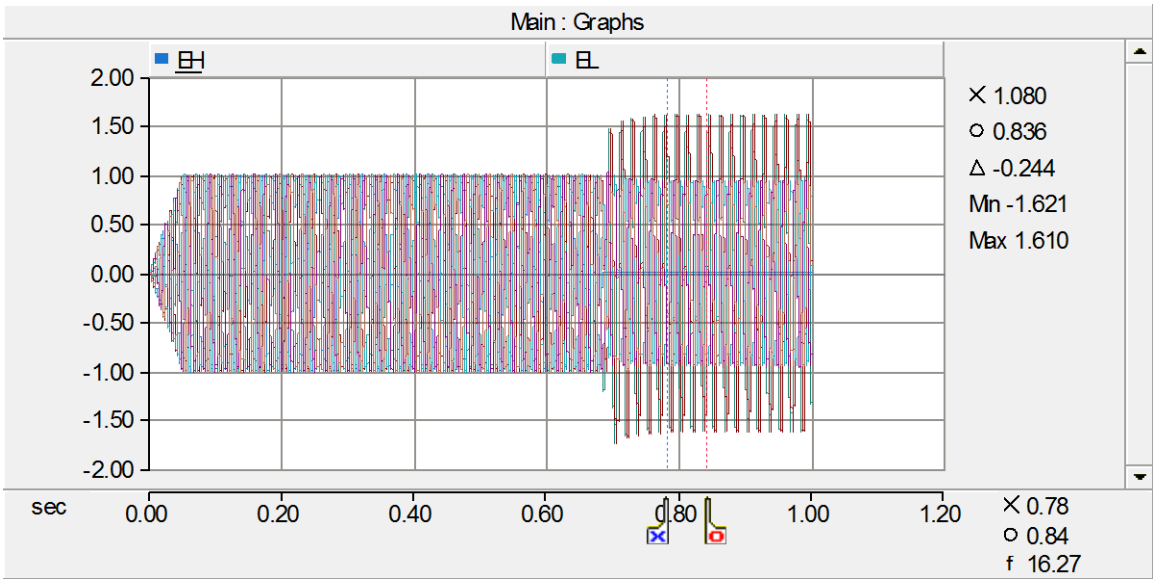
4.2.17. Scenario#17



Delta Side Voltage with 22KV MCOV Surge Arrester -AE 250 KW

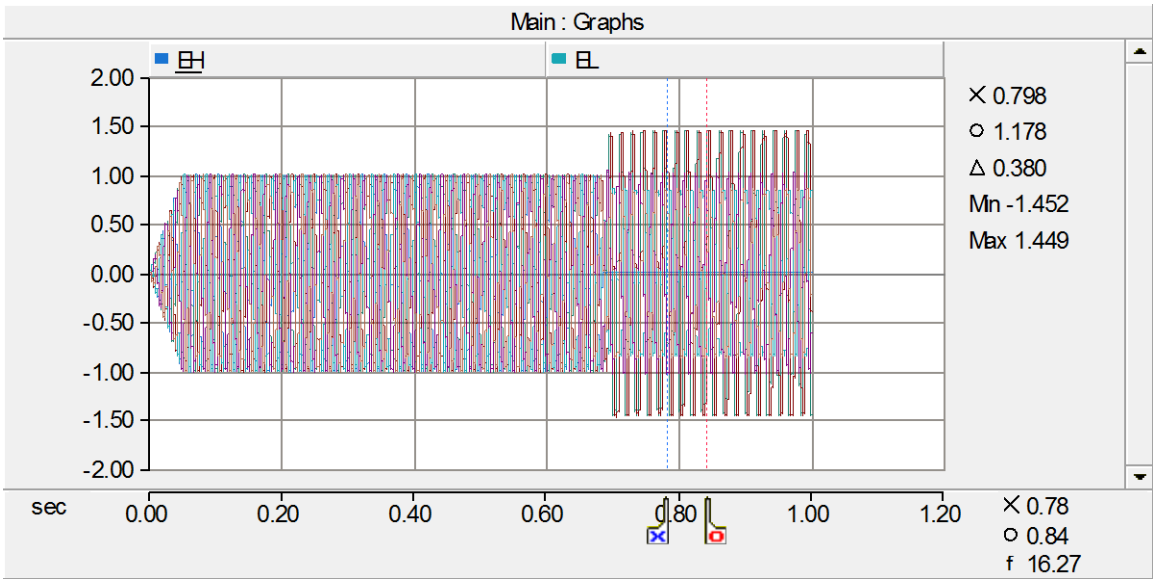


Delta Side Voltage with 24.4KV MCOV Surge Arrester -AE 250 KW

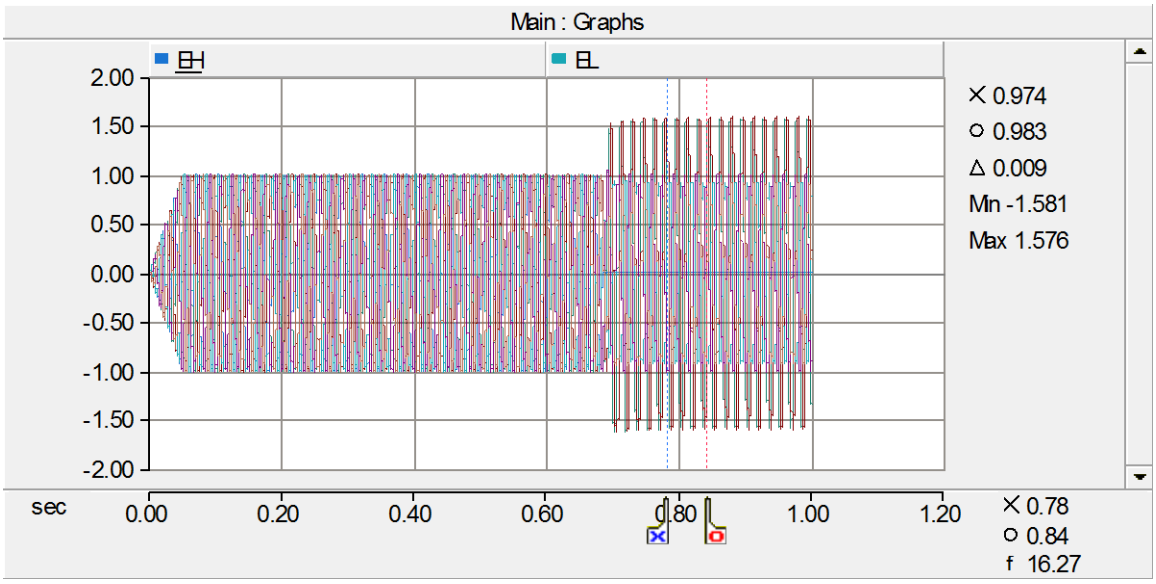


Delta Side Voltage with 29KV MCOV Surge Arrester -AE 250 KW

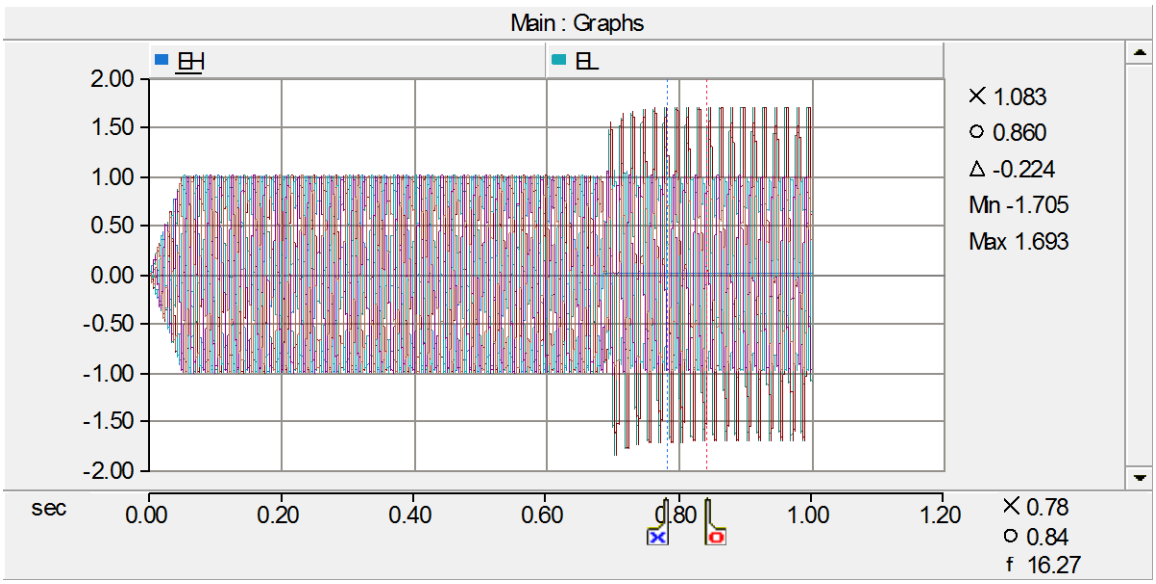
4.2.18. Scenario#18



Delta Side Voltage with 22KV MCOV Surge Arrester -AE 250 KW

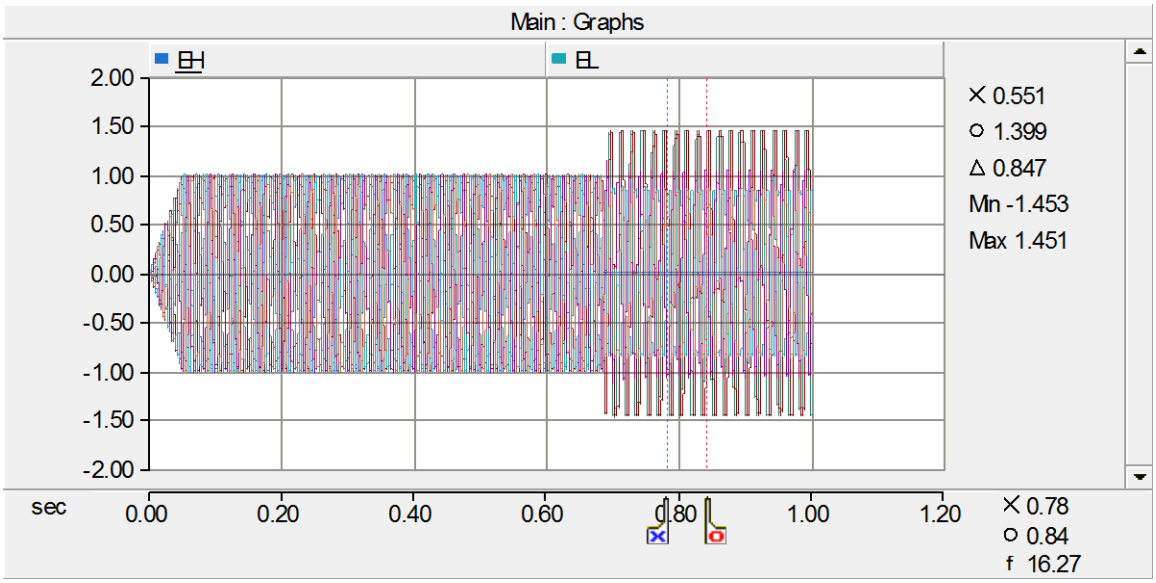


Delta Side Voltage with 24.4KV MCOV Surge Arrester -AE 250 KW

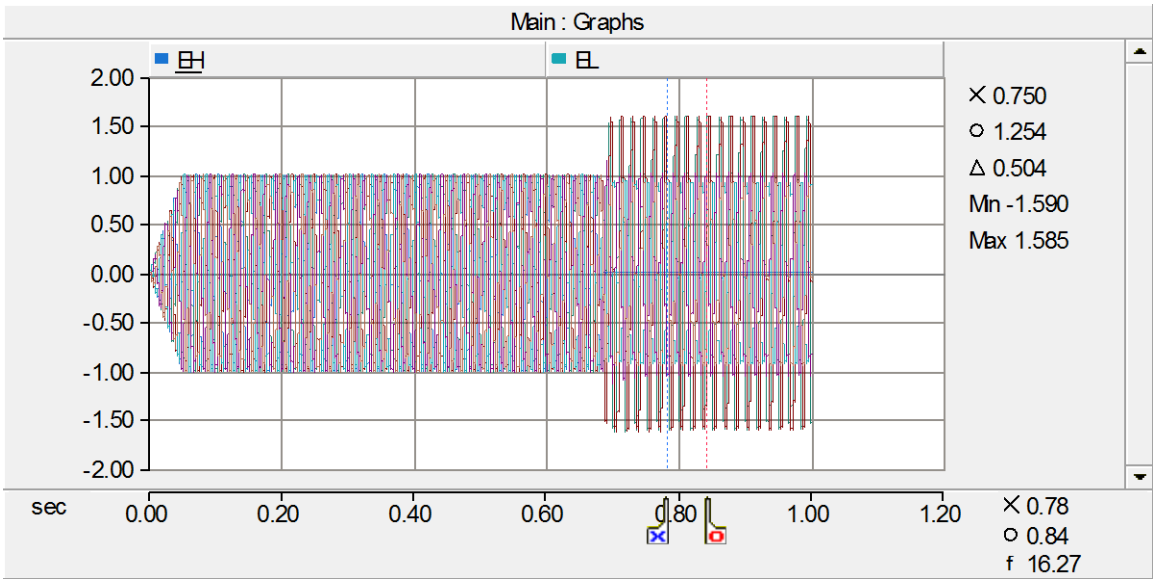


Delta Side Voltage with 29KV MCOV Surge Arrester -AE 250 KW

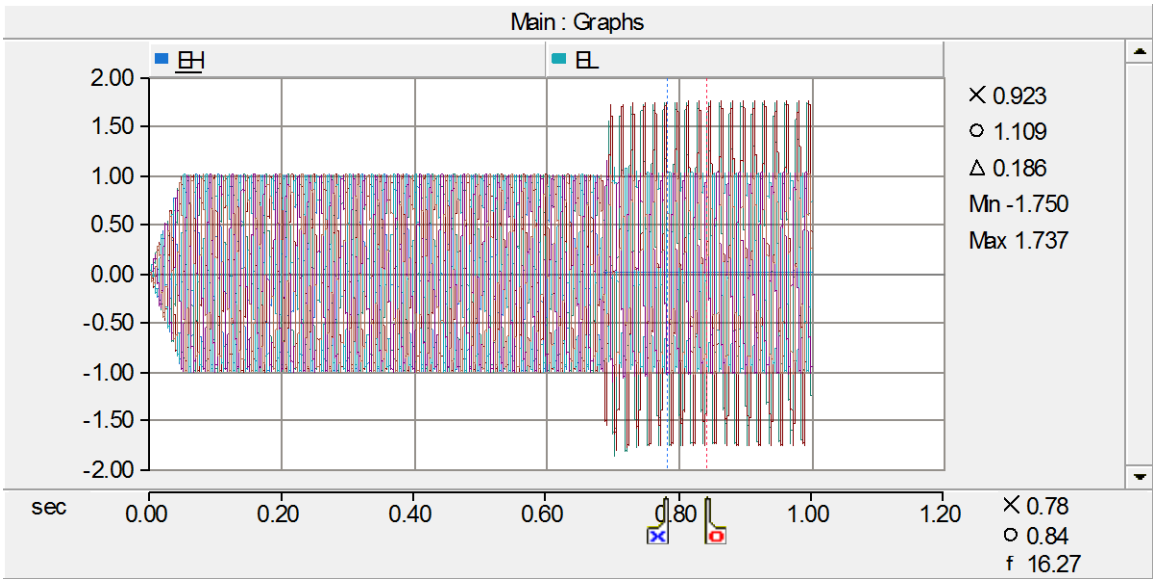
4.2.19. Scenario#19



Delta Side Voltage with 22KV MCOV Surge Arrester -AE 250 KW

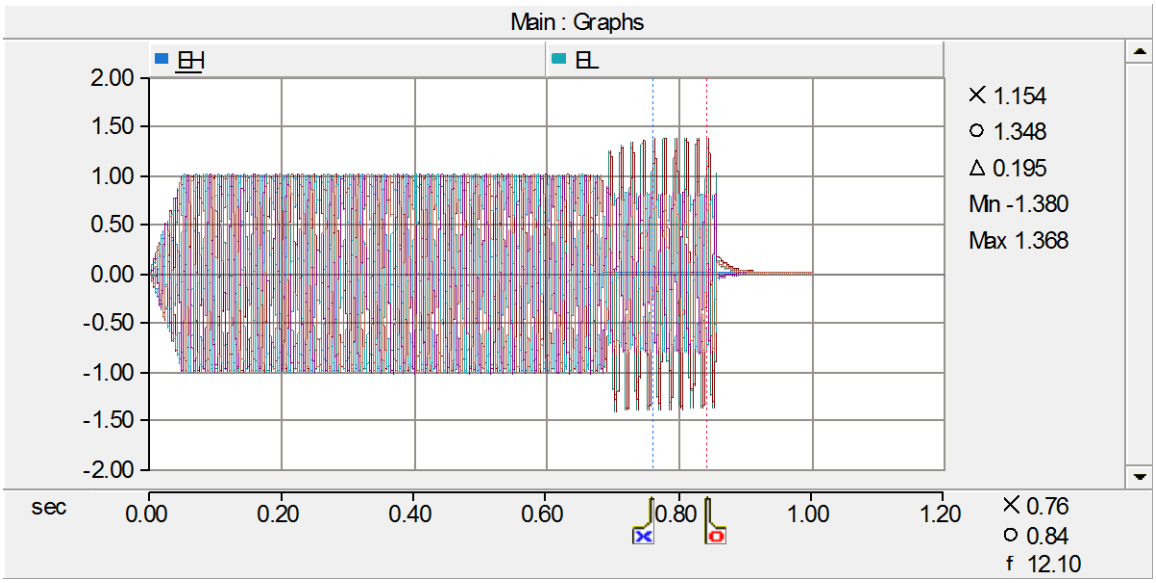


Delta Side Voltage with 24.4KV MCOV Surge Arrester -AE 250 KW

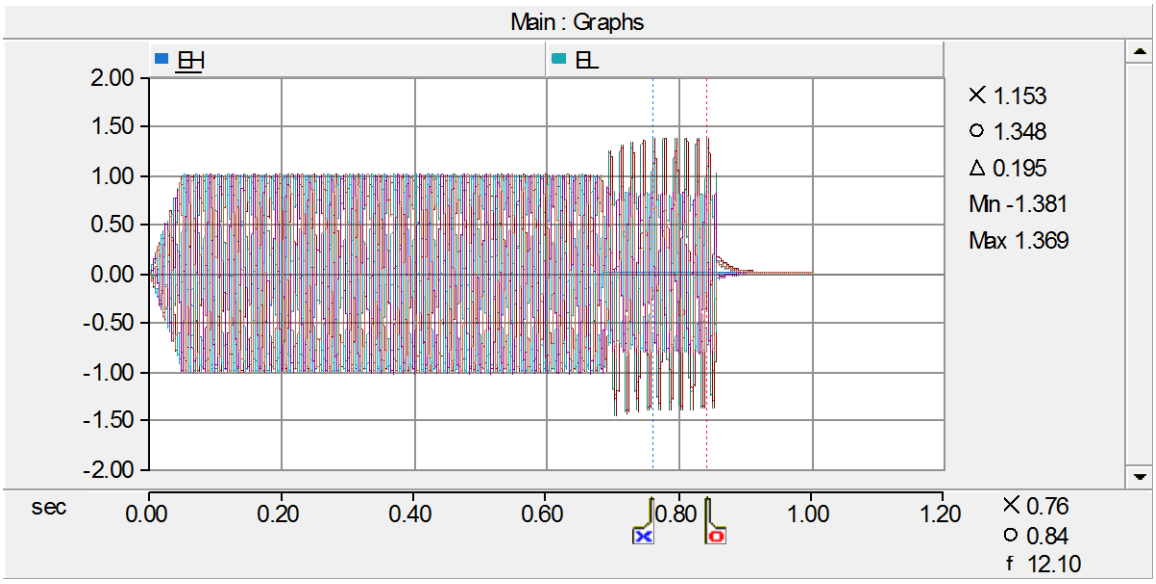


Delta Side Voltage with 29KV MCOV Surge Arrester -AE 250 KW

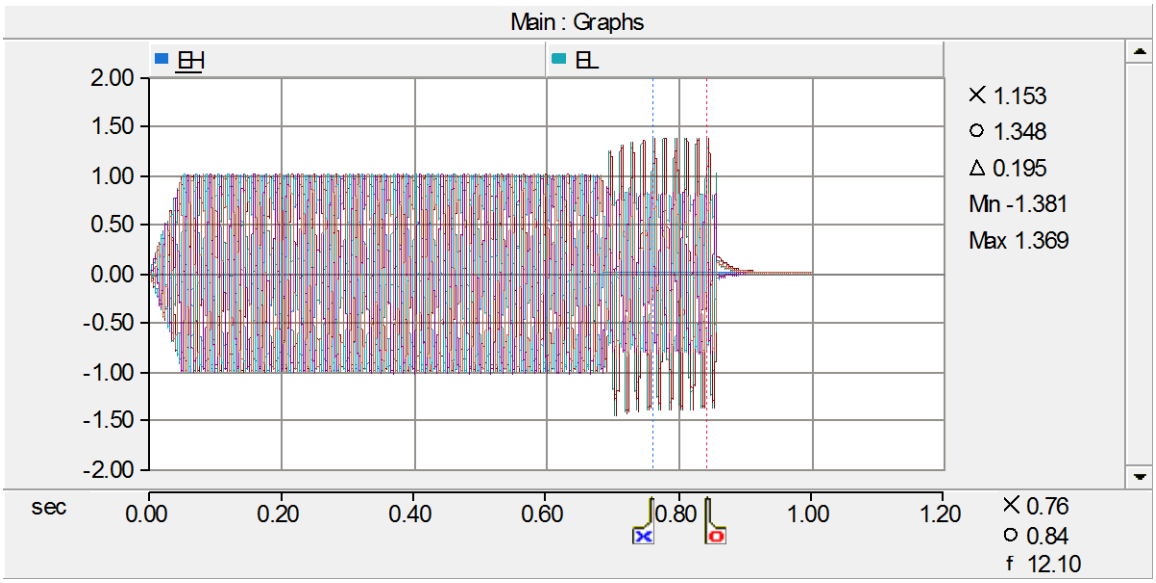
4.2.20. Scenario#20



Delta Side Voltage with 22KV MCOV Surge Arrester -AE 250 KW

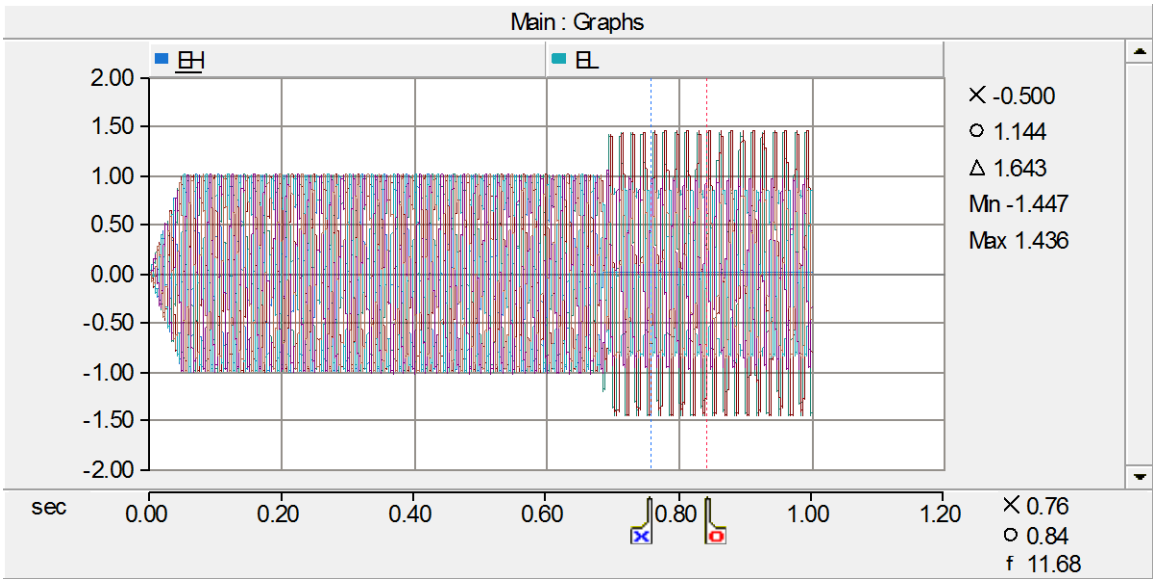


Delta Side Voltage with 24.4KV MCOV Surge Arrester -AE 250 KW

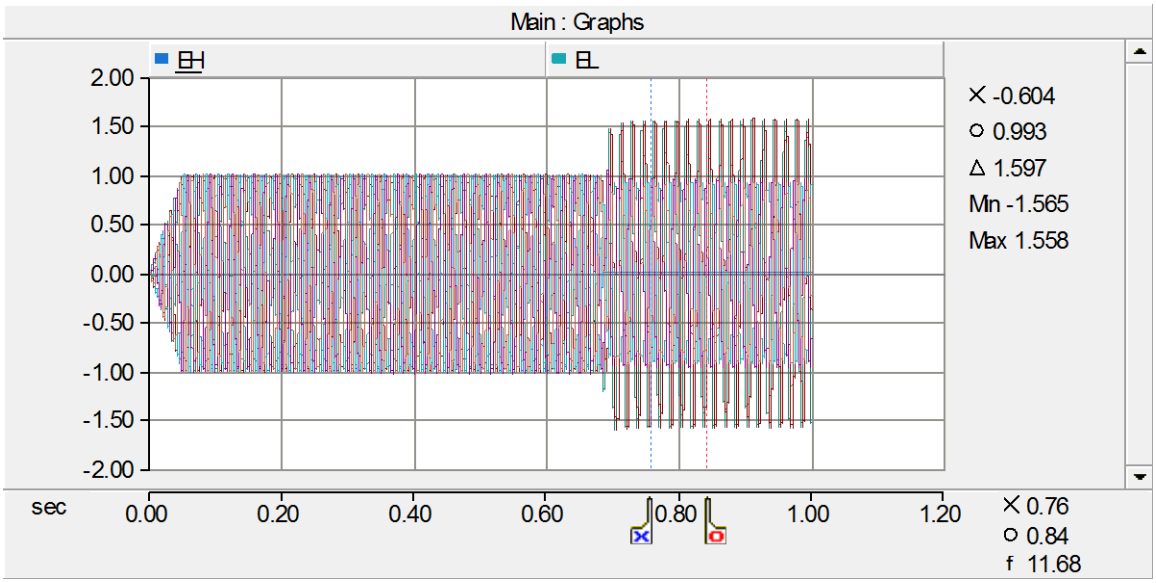


Delta Side Voltage with 29KV MCOV Surge Arrester -AE 250 KW

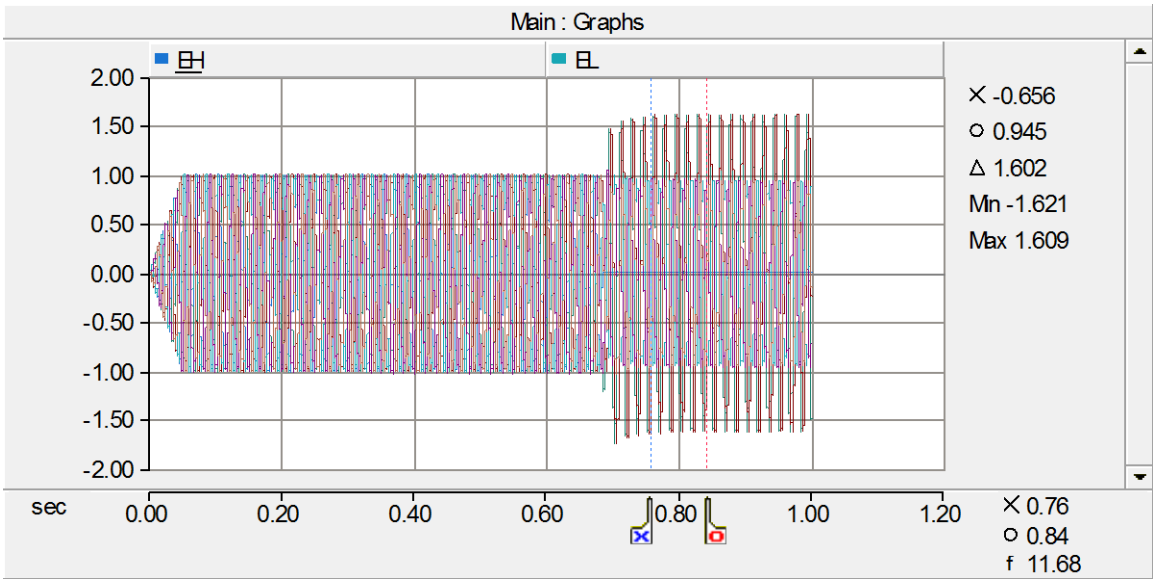
4.2.21. Scenario#21



Delta Side Voltage with 22KV MCOV Surge Arrester -AE 250 KW

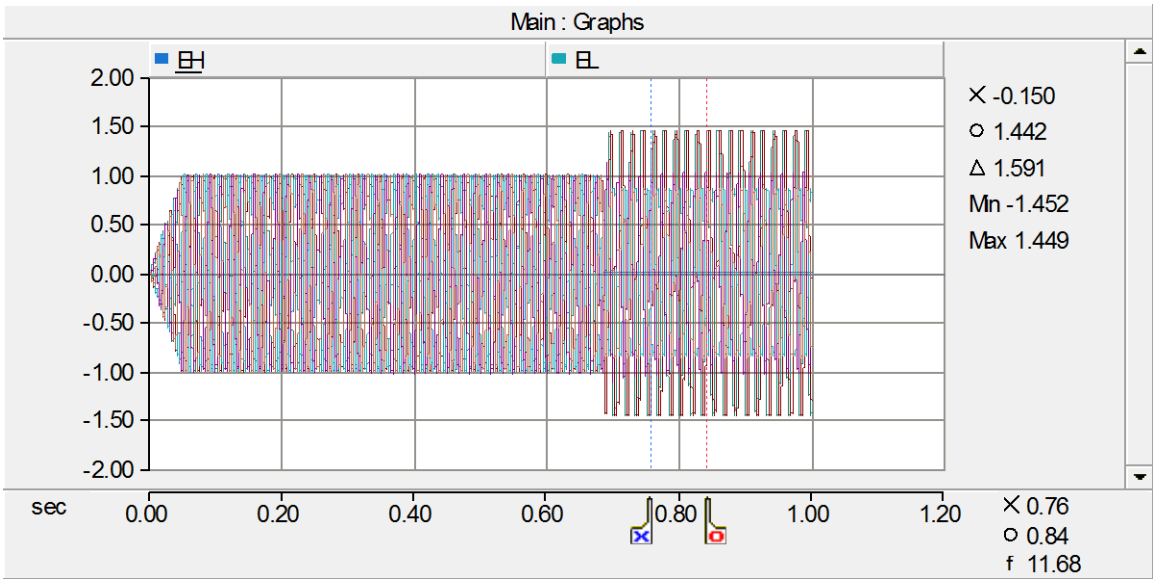


Delta Side Voltage with 24.4KV MCOV Surge Arrester -AE 250 KW

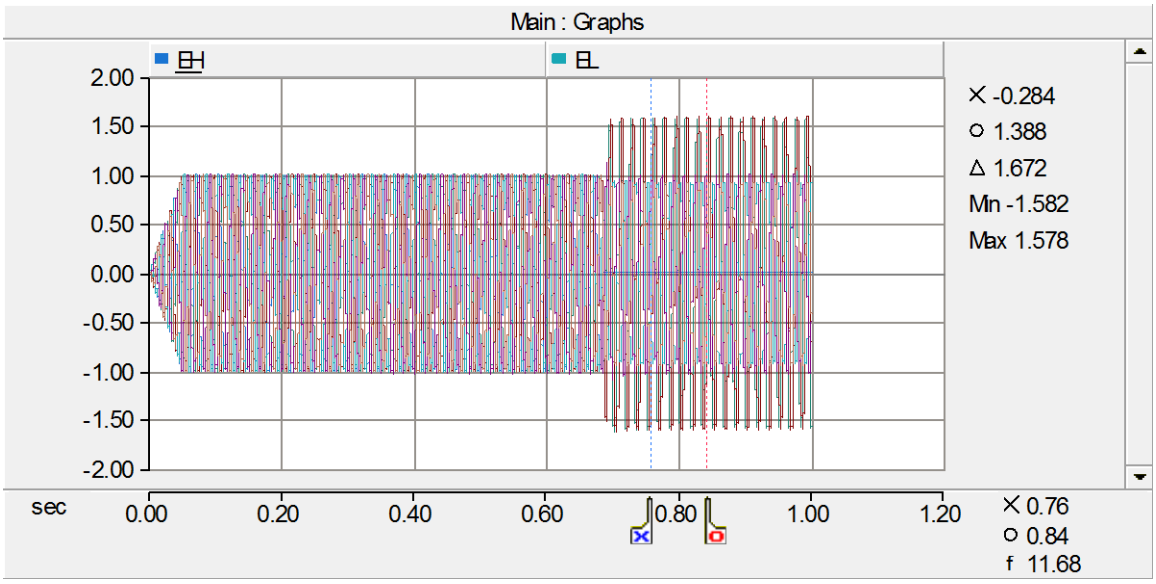


Delta Side Voltage with 29KV MCOV Surge Arrester -AE 250 KW

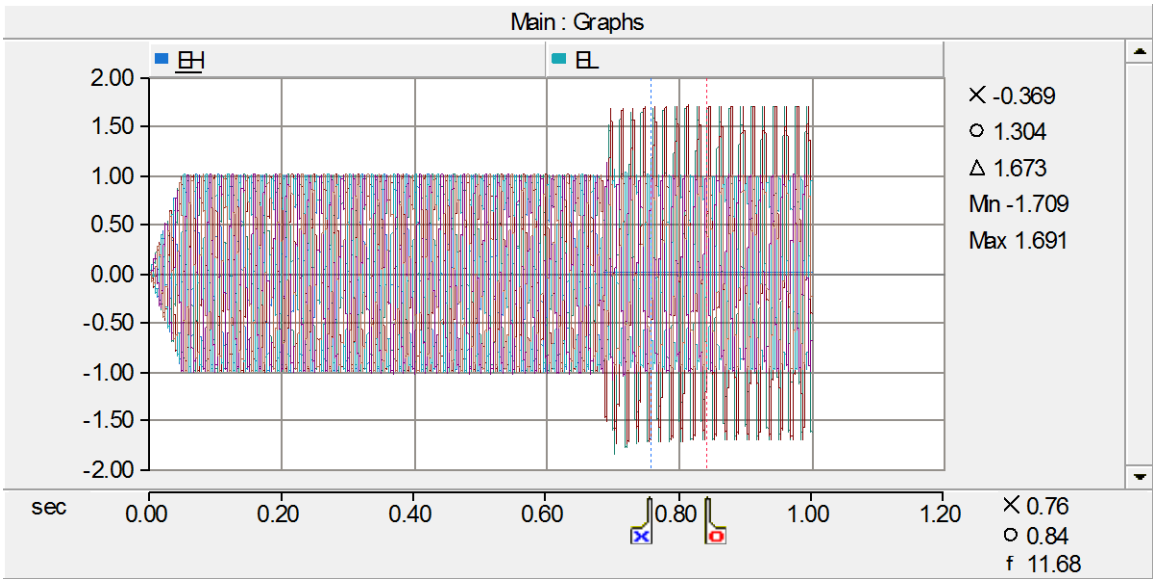
4.2.22. Scenario#22



Delta Side Voltage with 22KV MCOV Surge Arrester -AE 250 KW

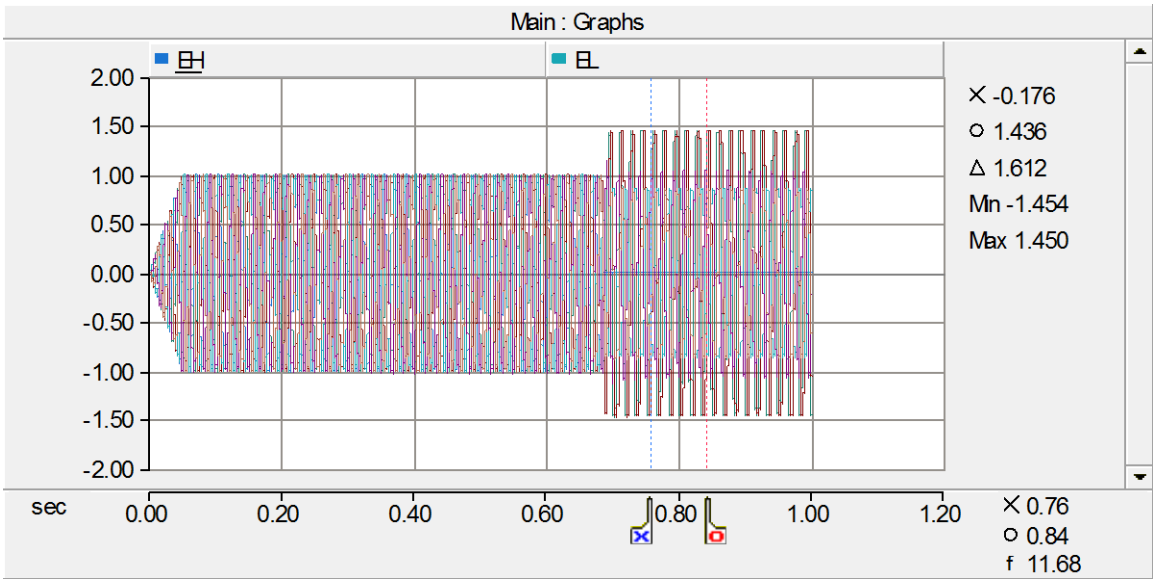


Delta Side Voltage with 24.4KV MCOV Surge Arrester -AE 250 KW

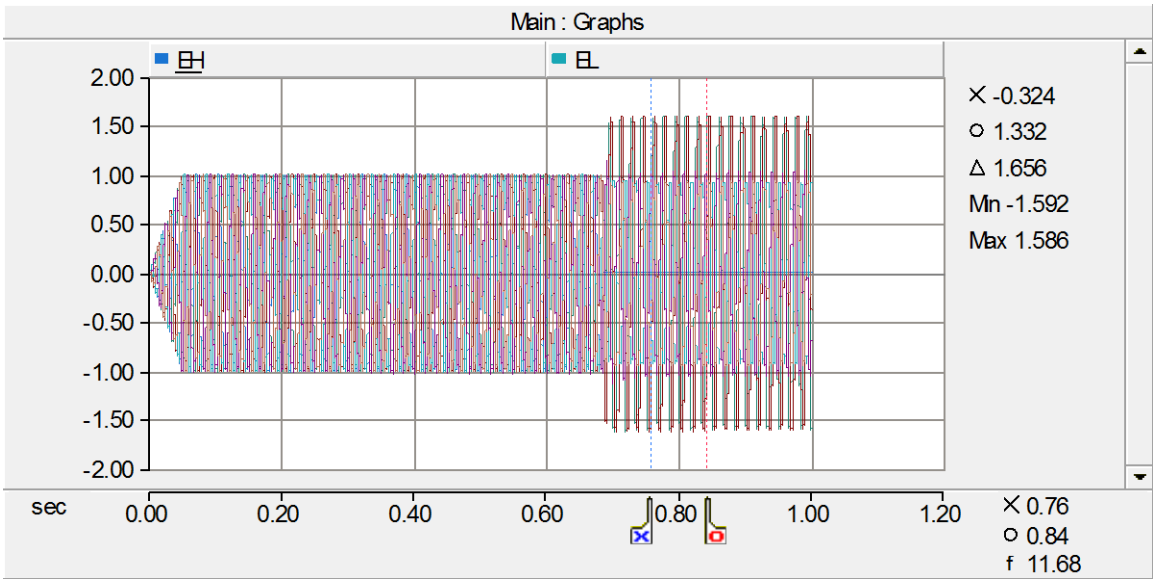


Delta Side Voltage with 29KV MCOV Surge Arrester -AE 250 KW

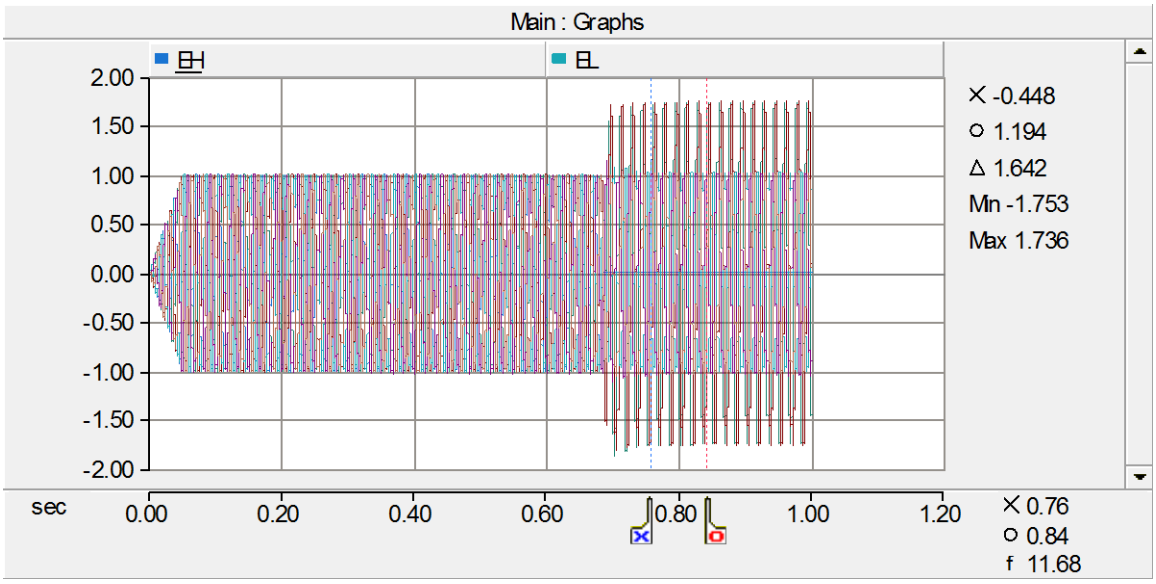
4.2.23. Scenario#23



Delta Side Voltage with 22KV MCOV Surge Arrester -AE 250 KW

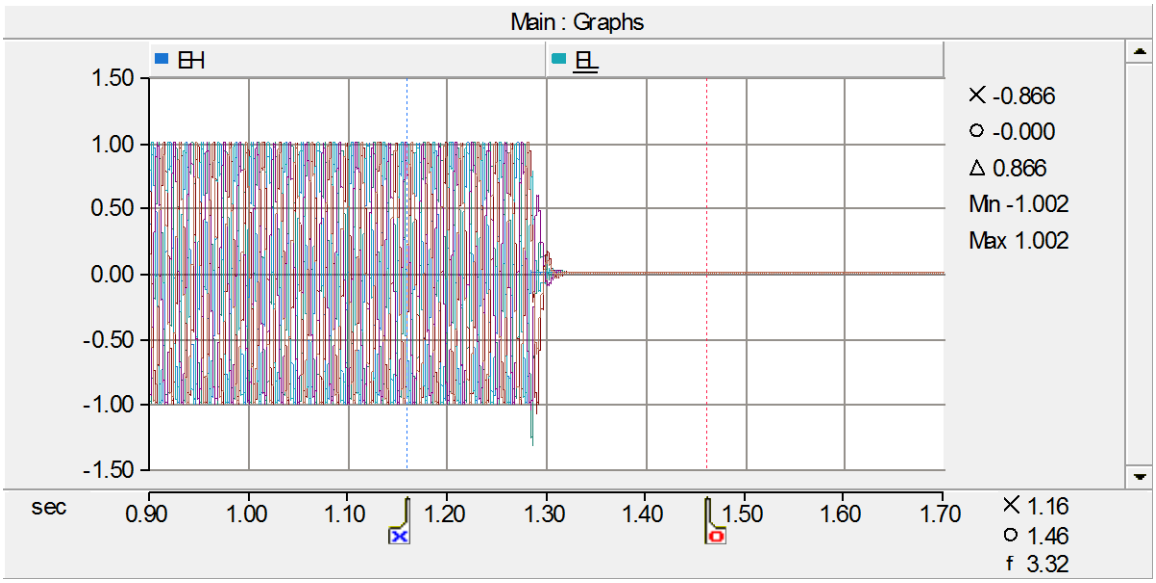


Delta Side Voltage with 24.4KV MCOV Surge Arrester -AE 250 KW



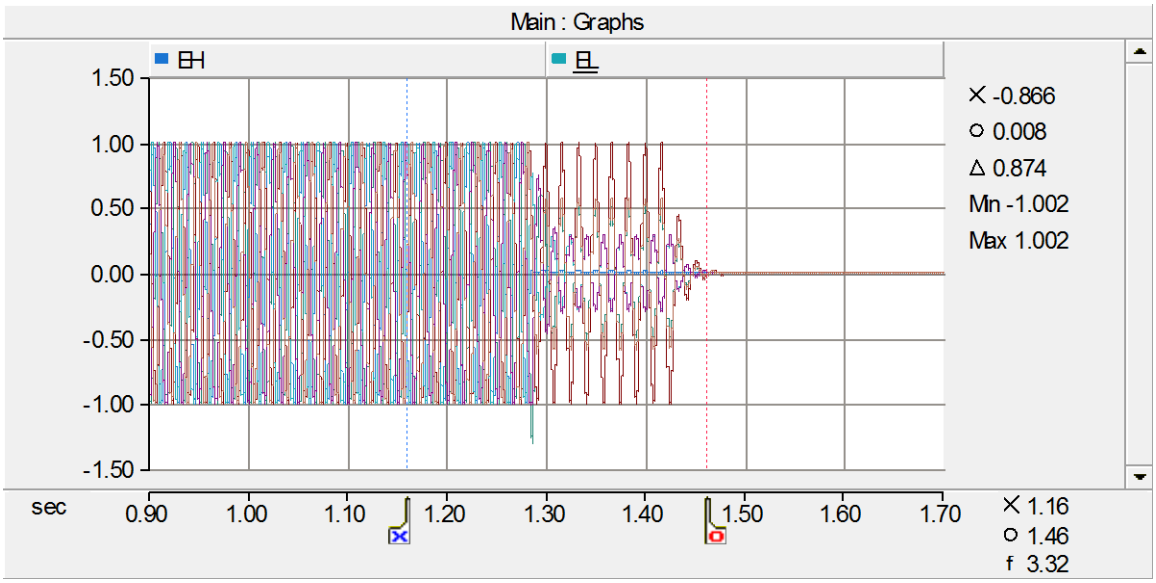
Delta Side Voltage with 29KV MCOV Surge Arrester -AE 250 KW

4.2.24. Scenario#24



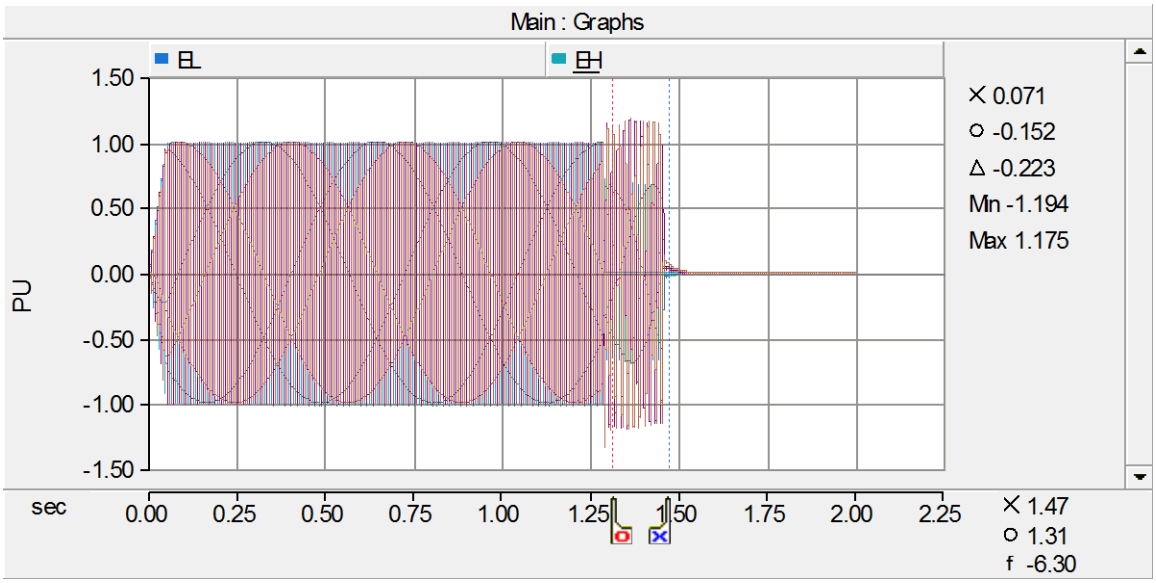
Delta Side Voltage with Inverter#2; Load Quality Factor Equal to 1

4.2.25. Scenario#25

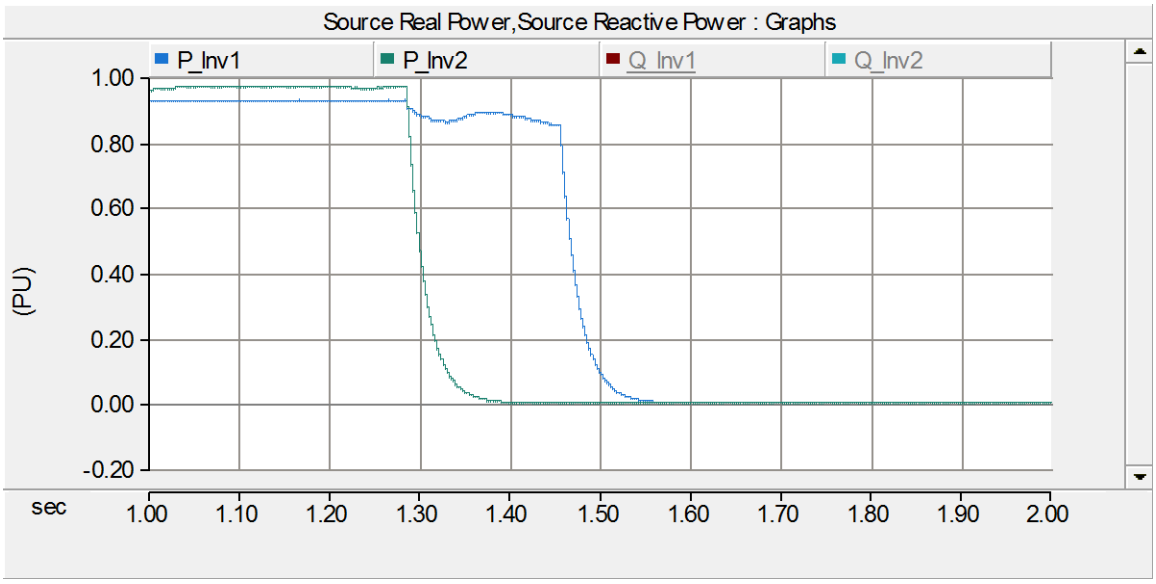


Delta Side Voltage with Inverter#2; Load Quality Factor Equal to 2.5

4.2.26. Scenario#26

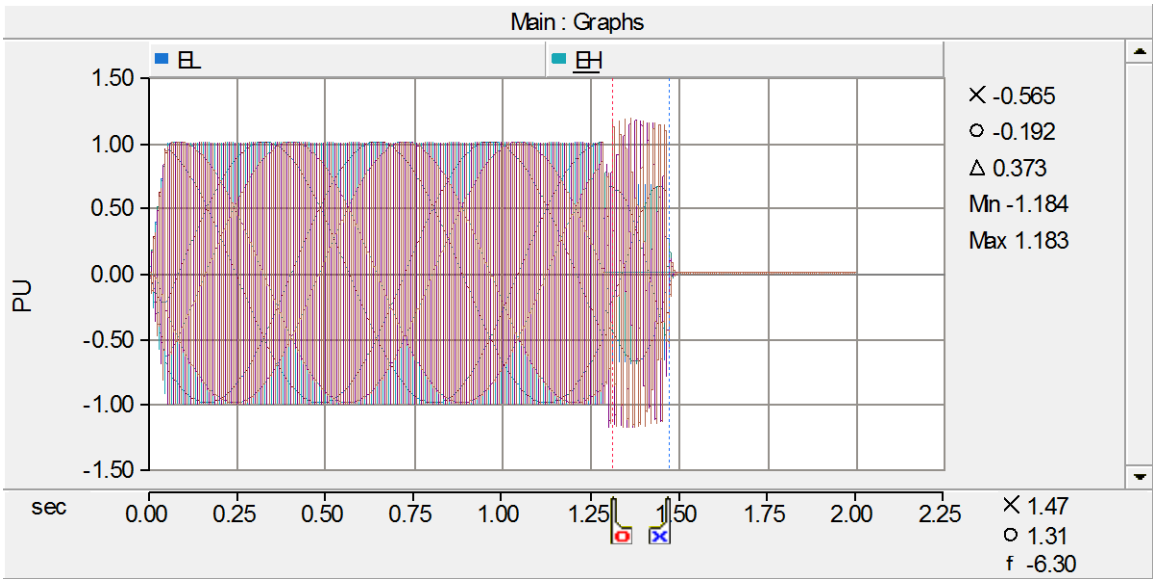


Delta Side Voltage with Combination of Inverter#1 and Inverter#2; Load with High Quality Factor is Out of Service

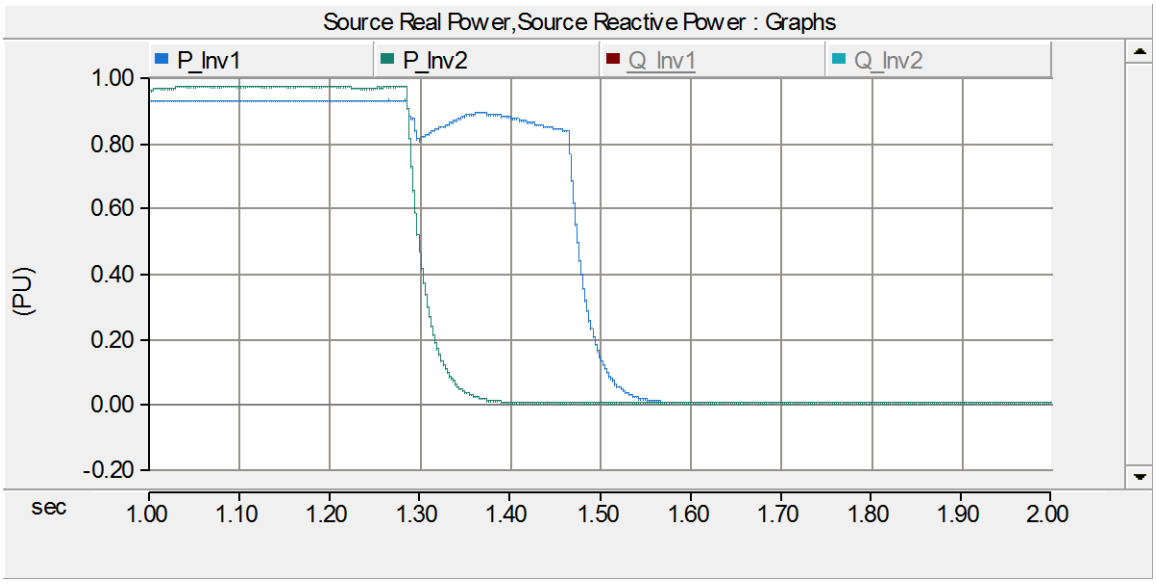


Output of Inverter#1 and Inverter#2; Load with High Quality Factor is Out of Service

4.2.27. Scenario#27

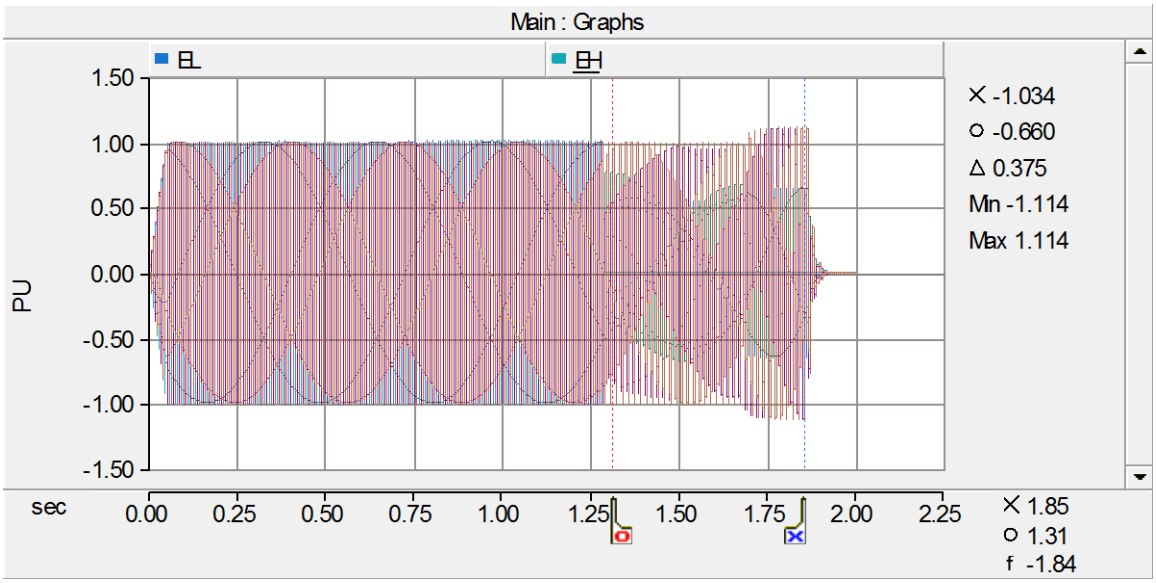


Delta Side Voltage with Combination of Inverter#1 and Inverter#2; Load Quality Factor Equal to 1

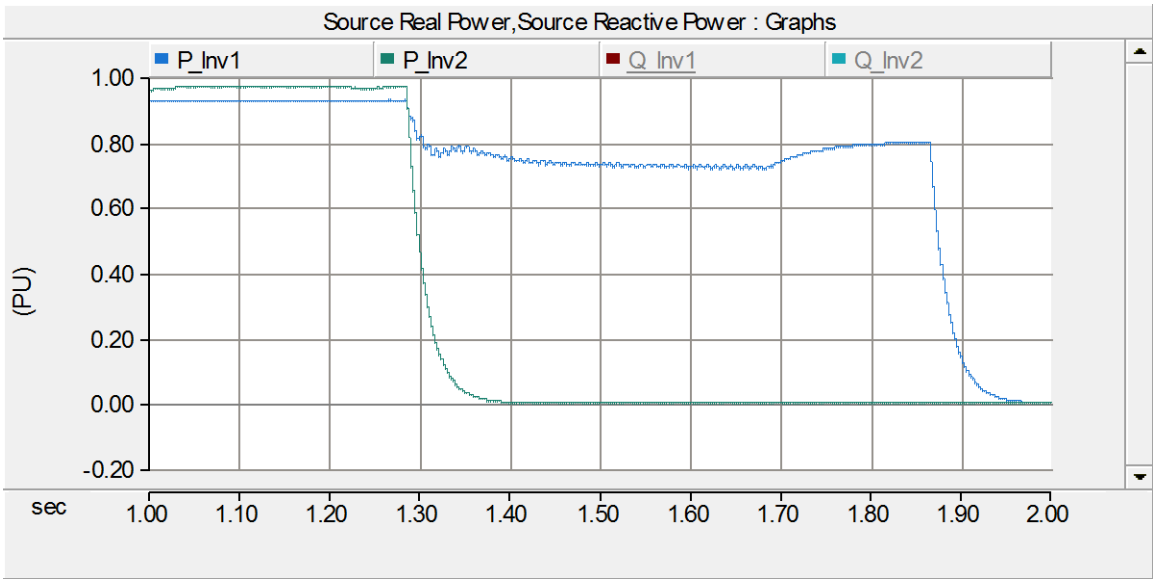


Output of Inverter#1 and Inverter#2; Load Quality Factor Equal to 1

4.2.28. Scenario#28



Delta Side Voltage with Combination of Inverter#1 and Inverter#2; Load Quality Factor Equal to 2.5



Output of Inverter#1 and Inverter#2; Load Quality Factor Equal to 2.5